

Compal Confidential

NCQD0 M/B Schematics Document

Intel Arrandale/Clarkfield Processor with DDRIII + Ibex Peak-M

2009-08-10

REV:1.0

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Issued Date	2009/08/10	Deciphered Date	2010/08/10	Title	SCHEMATICS,MB A5511
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				Document Number	401762
Date: Tuesday, August 18, 2009				Sheet	1 of 60

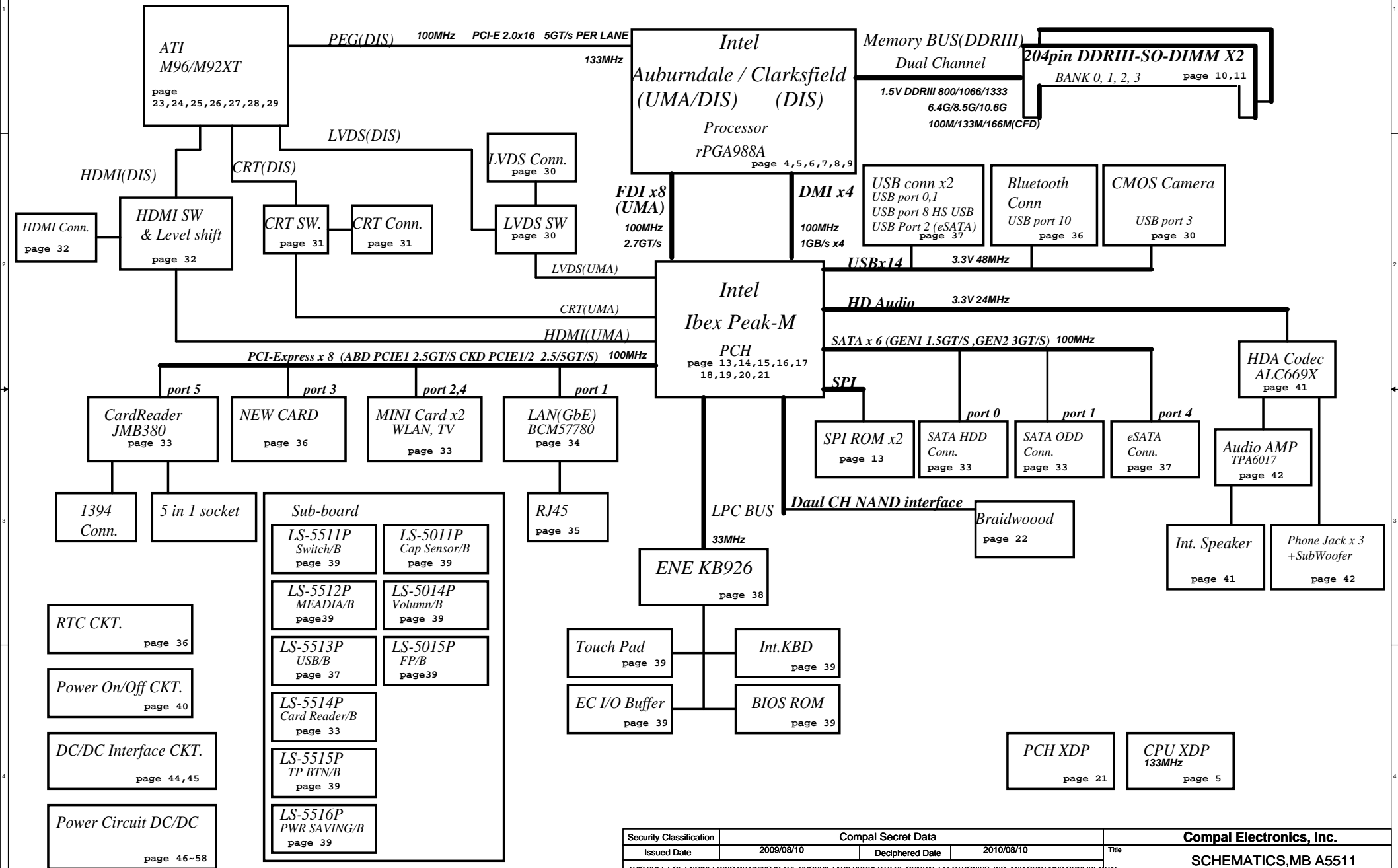
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Model Name : NCQD0

File Name : LA5511P

Fan Control
page 43

Clock Generator
IDT: 9LRS3199AKLFT
SILEGO: SLG8SP587
133/120/100/96/14.318MHZ to PCH
48MHZ to CardReader
page 12



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Voltage Rails

Power Plane	Description	S1	S3	S5	DGPU (UMA)	DGPU (DIS)
VIN	Adapter power supply (19V)	N/A	N/A	N/A		
B+	AC or battery power rail for power circuit.	N/A	N/A	N/A		
+CPU_CORE	Core voltage for CPU	ON	ON	OFF		
+0.75VS	0.75V switched power rail for DDR terminator	ON	OFF	OFF		
+1.05VS	1.05V switched power rail for PCH	ON	OFF	OFF		
+1.1VS_VTT	1.1V switched power rail (1.05 for AUB CPU)	ON	OFF	OFF		
+1.5V	1.5V power rail for DDRIII	ON	ON	OFF		
+1.5VS	1.5V switched power rail	ON	OFF	OFF		
+1.8VS	1.8V switched power rail	ON	OFF	OFF		
+3VALW	3.3V always on power rail	ON	ON	ON*		
+3V	3.3V power rail for PCH	ON	ON	ON		
+3V_LAN	3.3V power rail for LAN	ON	ON	ON*		
+3VS	3.3V switched power rail	ON	OFF	OFF		
+5VALW	5V always on power rail	ON	ON	ON*		
+5VS	5V switched power rail	ON	OFF	OFF		
+5V	5V power rail for PCH	ON	ON	ON		
+VSB	VSB always on power rail	ON	ON	ON*		
+RTCVCC	RTC power	ON	ON	ON		
+5VSDGPU	5V power rail for GPU				OFF	ON
+1.5VSDGPU	1.5V power rail for VRAM				OFF	ON
+1.8VSDGPU	1.8V switched power rail for GPU				OFF	ON

Note : ON* means that this power plane is ON only with AC power available, otherwise it is OFF.

External PCI Devices

Device	IDSEL#	REQ#/GNT#	Interrupts
--------	--------	-----------	------------

EC SM Bus1 address

Device	Address	Device	Address
Smart Battery	0001 011X b		

EC SM Bus2 address

Ibex SM Bus address

Device	Address
Clock Generator (9LRS3199AKLFT, SLG8SP587)	1101 0010b
DDR DIMM0	1001 000Xb
DDR DIMM2	1001 010Xb
ISL90727	0101 1100b
ISL90728	0111 1100b

STATE	SIGNAL	SLP_S1#	SLP_S3#	SLP_S4#	SLP_S5#	+VALW	+V	+VS	Clock
Full ON		HIGH	HIGH	HIGH	HIGH	ON	ON	ON	ON
S1(Power On Suspend)		LOW	HIGH	HIGH	HIGH	ON	ON	ON	LOW
S3 (Suspend to RAM)		LOW	LOW	HIGH	HIGH	ON	ON	OFF	OFF
S4 (Suspend to Disk)		LOW	LOW	LOW	HIGH	ON	OFF	OFF	OFF
S5 (Soft OFF)		LOW	LOW	LOW	LOW	ON	OFF	OFF	OFF

Board ID / SKU ID Table for AD channel

Vcc	3.3V +/- 5%			
Ra/Rc/Re	100K +/- 5%			
Board ID	Rb / Rd / Rf	VAD_BID min	VAD_BID typ	VAD_BID max
0		0 V	0 V	0 V
1	8.2K +/- 5%	0.216 V	0.250 V	0.289 V
2	18K +/- 5%	0.436 V	0.503 V	0.538 V
3	33K +/- 5%	0.712 V	0.819 V	0.875 V
4	56K +/- 5%	1.036 V	1.185 V	1.264 V
5	100K +/- 5%	1.453 V	1.650 V	1.759 V
6	200K +/- 5%	1.935 V	2.200 V	2.341 V
7	NC	2.500 V	3.300 V	3.300 V

BOARD ID Table

Board ID	PCB Revision
* 0	0.1
1	
2	
3	
4	
5	
6	
7	

BTO Option Table

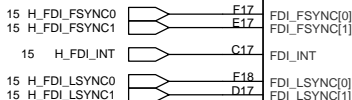
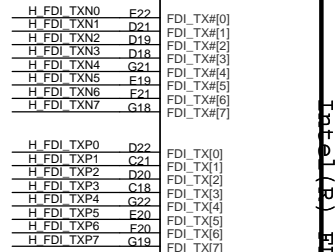
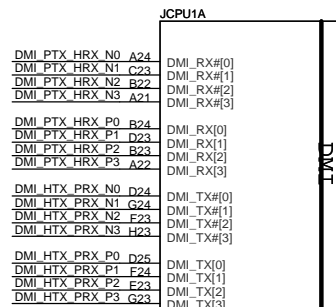
BTO Item	BOM Structure
UMA	UMA@
UMA Only	UMAO@
DIS Only	DIS@
DGPU	VGA@
Braidwood	NV@
M96	M96@
Broadway	MAD@
Switchable Graphics	SG@

USB Port Table

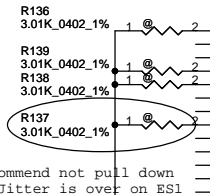
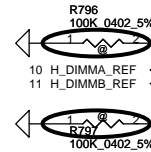
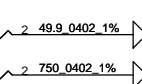
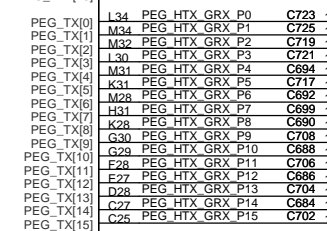
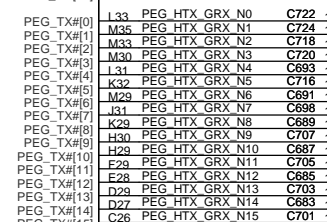
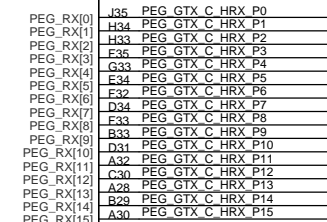
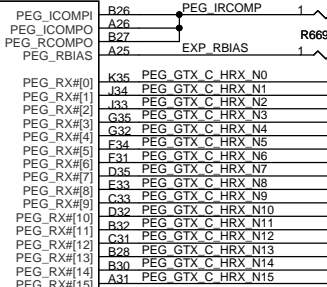
USB 2.0	USB 1.1	Port	4 External USB Port
EHCI1	UHCI0	0	USB Conn.
		1	USB/B
	UHCI1	2	eSATA USB
		3	CMOS Camera
	UHCI2	4	Mini Card 1
		5	Mini Card 2
		6	
EHCI2	UHCI3	7	
	UHCI4	8	USB Conn.
		9	
	UHCI5	10	Blue Tooth
		11	Finger Print
	UHCI6	12	NewCard
		13	

BOM Config
Switchable Graphics (M96)SKU: UMA@/SG@/VGA@
UMA only SKU: UMA@/UMAO@
DIS ONLY (M96): DIS@/VGA@

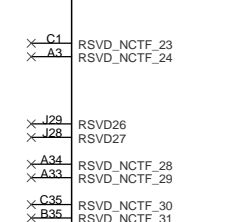
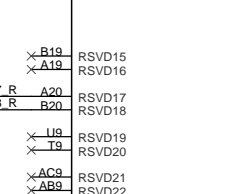
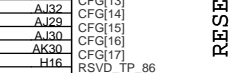
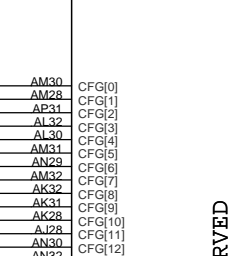
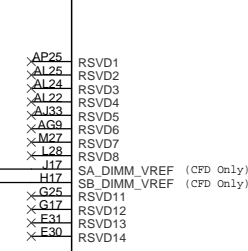
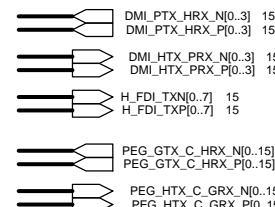
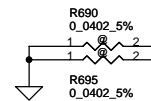
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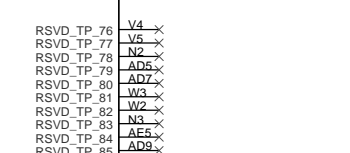
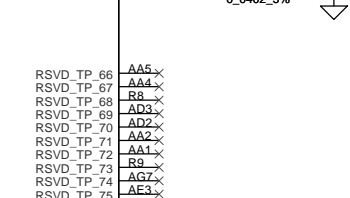
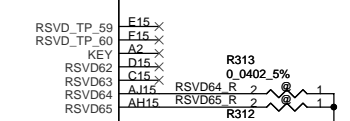
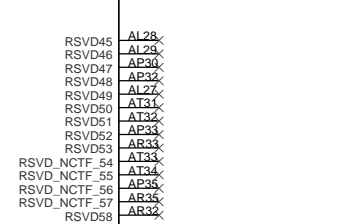
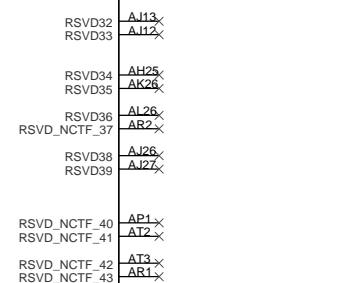
IC:AUB_CFD_rPGA,R1P0
CONN@



WW41 Recommend not pull down
PCIE2.0 Jitter is over on ES1



IC:AUB_CFD_rPGA,R1P0
CONN@

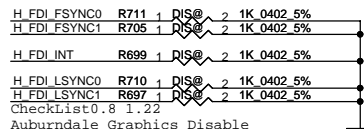


VSS

AP34

eDP Signals MAPPING

eDP Signal	PEG Singals	Lane Reversal
eDP_TX0	PEG HTX_C_GRX_P15	PEG HTX_C_GRX_P0
eDP_TX#0	PEG HTX_C_GRX_N15	PEG HTX_C_GRX_N0
eDP_TX1	PEG HTX_C_GRX_P14	PEG HTX_C_GRX_P1
eDP_TX#1	PEG HTX_C_GRX_N14	PEG HTX_C_GRX_N1
eDP_TX2	PEG HTX_C_GRX_P13	PEG HTX_C_GRX_P2
eDP_TX#2	PEG HTX_C_GRX_N13	PEG HTX_C_GRX_N2
eDP_TX3	PEG HTX_C_GRX_P12	PEG HTX_C_GRX_P3
eDP_TX#3	PEG HTX_C_GRX_N12	PEG HTX_C_GRX_N3
eDP_AUX	PEG GTX_C_HRX_P13	PEG GTX_C_HRX_P2
eDP_AUX#	PEG GTX_C_HRX_N13	PEG GTX_C_HRX_N2
eDP_HTX_C_GRX_P1	PEG GTX_C_HRX_P1	PEG GTX_C_HRX_P3
eDP_HTX_C_GRX_N1	PEG GTX_C_HRX_N1	PEG GTX_C_HRX_N3



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10 DDR_A_D[0..63]
10 DDR_A_DM[0..7]
10 DDR_A_DQS[0..7]
10 DDR_A_MA[0..15]

DDR A D0 A10
DDR A D1 C10
DDR A D2 C7
DDR A D3 A7
DDR A D4 B10
DDR A D5 D10
DDR A D6 E10
DDR A D7 A8
DDR A D8 D8
DDR A D9 F10
DDR A D10 E6
DDR A D11 E7
DDR A D12 E9
DDR A D13 B7
DDR A D14 E7
DDR A D15 C6
DDR A D16 H10
DDR A D17 G8
DDR A D18 K7
DDR A D19 J8
DDR A D20 G7
DDR A D21 G10
DDR A D22 J7
DDR A D23 J10
DDR A D24 L7
DDR A D25 M6
DDR A D26 M8
DDR A D27 L9
DDR A D28 L6
DDR A D29 K8
DDR A D30 N8
DDR A D31 P9
DDR A D32 AH5
DDR A D33 AF5
DDR A D34 AK6
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DDR A D57 AN12
DDR A D58 AM13
DDR A D59 AT14
DDR A D60 AT12
DDR A D61 AL13
DDR A D62 AR14
DDR A D63 AP14

10 DDR_A_BS0
10 DDR_A_BS1
10 DDR_A_BS2

10 DDR_A_CAS#
10 DDR_A_RAS#
10 DDR_A_WE#

JCPU1C

SA_CK[0] AA6
SA_CK[1] AA7
SA_CKE[0] P7

SA_CK[1] Y6
SA_CK[1] Y6
SA_CKE[1] P6

SA_CS[0] AE2
SA_CS[1] AE8

SA_ODT[0] AD8
SA_ODT[1] AF9

SA_DM[0] B9
SA_DM[1] D7
SA_DM[2] H7
SA_DM[3] M7
SA_DM[4] AG6
SA_DM[5] AM7
SA_DM[6] AN10
SA_DM[7] AN13

SA_DQS[0] C9
SA_DQS[1] E8
SA_DQS[2] J8
SA_DQS[3] J9
SA_DQS[4] AH7
SA_DQS[5] AK9
SA_DQS[6] AP11
SA_DQS[7] AT13

SA_DQS[0] C8
SA_DQS[1] E9
SA_DQS[2] H9
SA_DQS[3] M9
SA_DQS[4] AH8
SA_DQS[5] AK10
SA_DQS[6] AN11
SA_DQS[7] AR13

SA_MA[0] Y3
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SA_MA[2] AA8
SA_MA[3] AA3
SA_MA[4] V1
SA_MA[5] AA9
SA_MA[6] V8
SA_MA[7] T1
SA_MA[8] Y9
SA_MA[9] U6
SA_MA[10] AD4
SA_MA[11] T2
SA_MA[12] U3
SA_MA[13] AG8
SA_MA[14] T3
SA_MA[15] V9

IC:AUB_CFD_rPGA,R1P0
CONN@

11 DDR_B_D[0..63]
11 DDR_B_DM[0..7]
11 DDR_B_DQS[0..7]
11 DDR_B_MA[0..15]

DDR B D0 B5
DDR B D1 A5
DDR B D2 C3
DDR B D3 B3
DDR B D4 E4
DDR B D5 A6
DDR B D6 C4
DDR B D7 D1
DDR B D8 D1
DDR B D9 D2
DDR B D10 F2
DDR B D11 E1
DDR B D12 C2
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DDR B D37 AG3
DDR B D38 AJ4
DDR B D39 AH4
DDR B D40 AK4
DDR B D41 AK3
DDR B D42 AM6
DDR B D43 AN2
DDR B D44 AK5
DDR B D45 AK2
DDR B D46 AM4
DDR B D47 AM3
DDR B D48 AP3
DDR B D49 AN5
DDR B D50 AT4
DDR B D51 AN6
DDR B D52 AN4
DDR B D53 AN3
DDR B D54 AT5
DDR B D55 AT6
DDR B D56 AN7
DDR B D57 AP6
DDR B D58 AP8
DDR B D59 AT9
DDR B D60 AT7
DDR B D61 AP9
DDR B D62 AR10
DDR B D63 AT10

11 DDR_B_BS0
11 DDR_B_BS1
11 DDR_B_BS2

11 DDR_B_CAS#
11 DDR_B_RAS#
11 DDR_B_WE#

JCPU1D

SB_DQ[0] W8
SB_CK[0] W9
SB_CKE[0] M3
SB_CK[1] V7
SB_CK[1] V7
SB_CKE[1] M2
SB_CS[0] AB8
SB_CS[1] AD6
SB_ODT[0] AC7
SB_ODT[1] AD1
SB_DM[0] D4
SB_DM[1] E1
SB_DM[2] H3
SB_DM[3] K1
SB_DM[4] AH1
SB_DM[5] AL2
SB_DM[6] AR4
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SB_MA[3] V3
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SB_MA[5] R2
SB_MA[6] R6
SB_MA[7] R4
SB_MA[8] R5
SB_MA[9] AR5
SB_MA[10] P3
SB_MA[11] R3
SB_MA[12] AF7
SB_MA[13] P5
SB_MA[14] N1

DDR_B_CLK0 11
DDR_B_CLK0# 11
DDR_B_CKE0 11

DDR_B_CLK1 11
DDR_B_CLK1# 11
DDR_B_CKE1 11

DDR_B_CS0# 11
DDR_B_CS1# 11

DDR_B_ODT0 11
DDR_B_ODT1 11

DDR_B_DM0
DDR_B_DM1
DDR_B_DM2
DDR_B_DM3
DDR_B_DM4
DDR_B_DM5
DDR_B_DM6
DDR_B_DM7

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DDR_B_DQS#2
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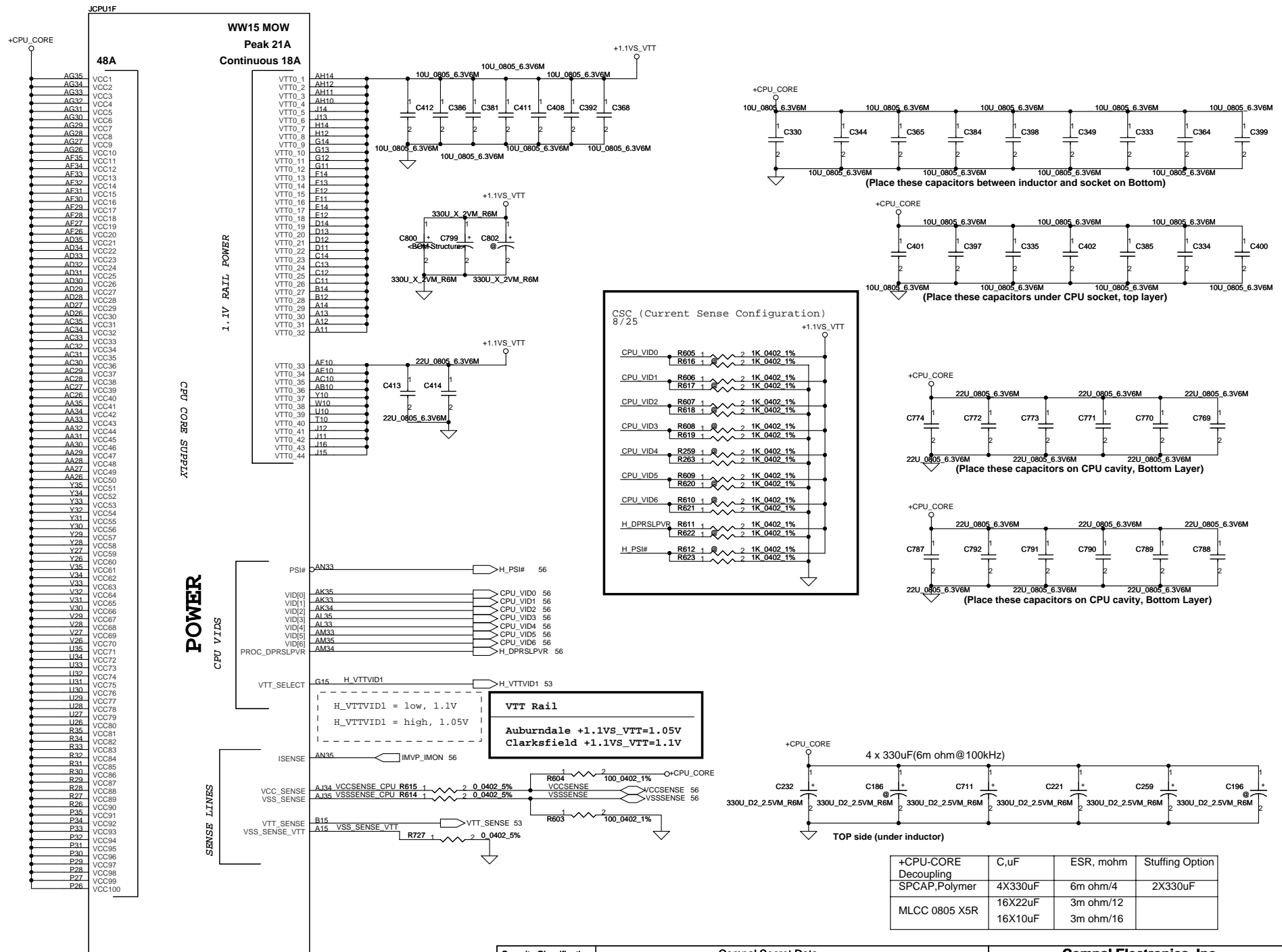
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DDR_B_MA6
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DDR_B_MA8
DDR_B_MA9
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DDR_B_MA15

DDR SYSTEM MEMORY - B

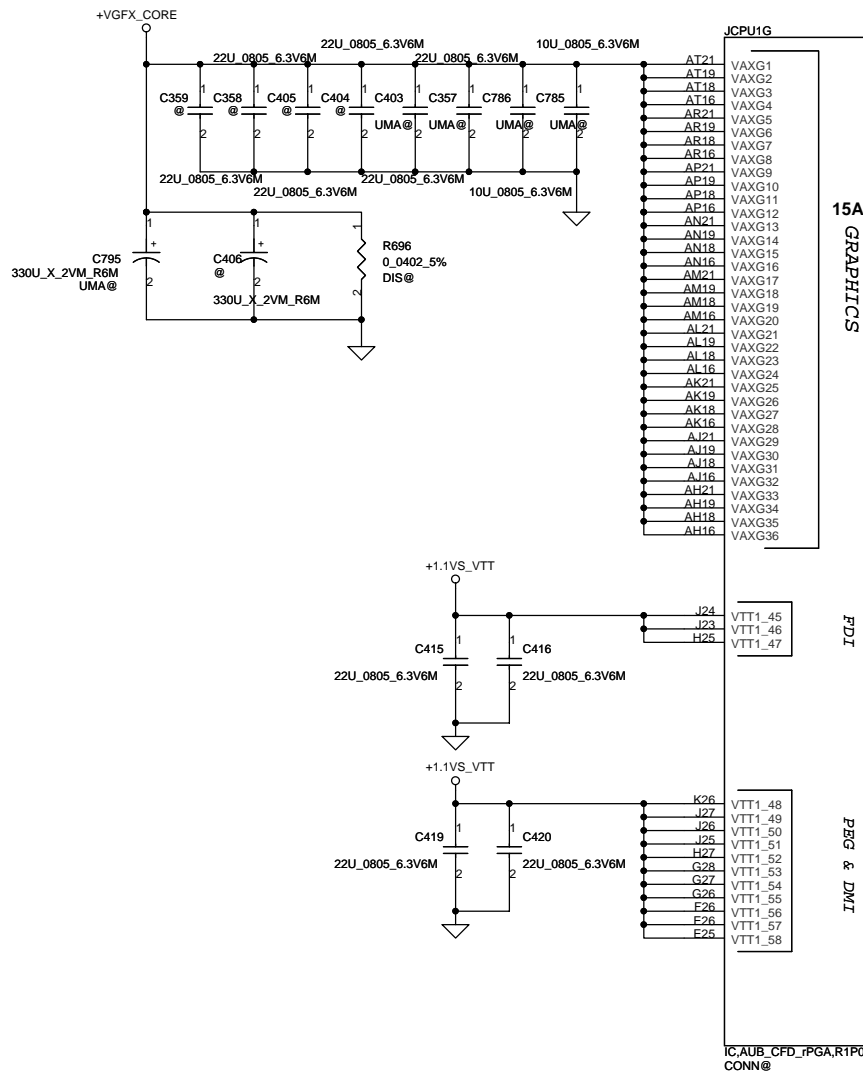
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IC,AUB_CFD_PGA,R1P0
CONN@

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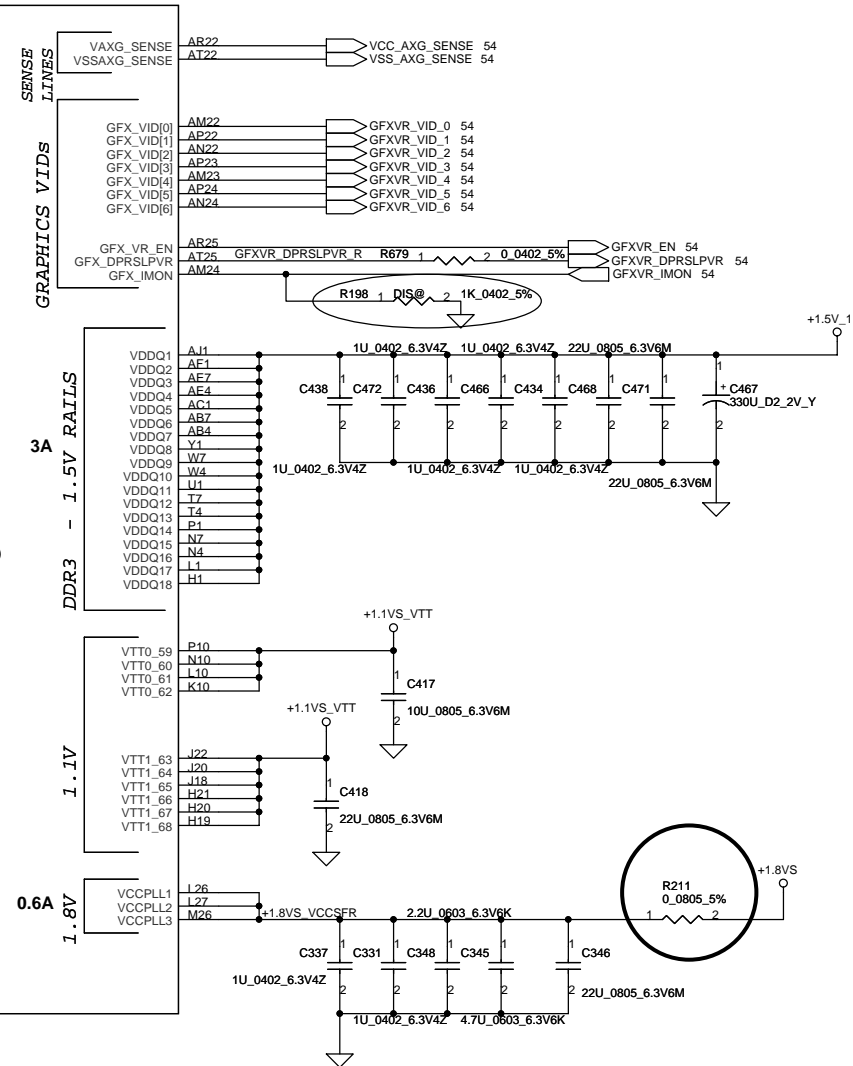
15A
GRAPHICS

POWER

FDI

PEG & DMI

IC:AUB_CFD_rPGA,R1P0
CONN@

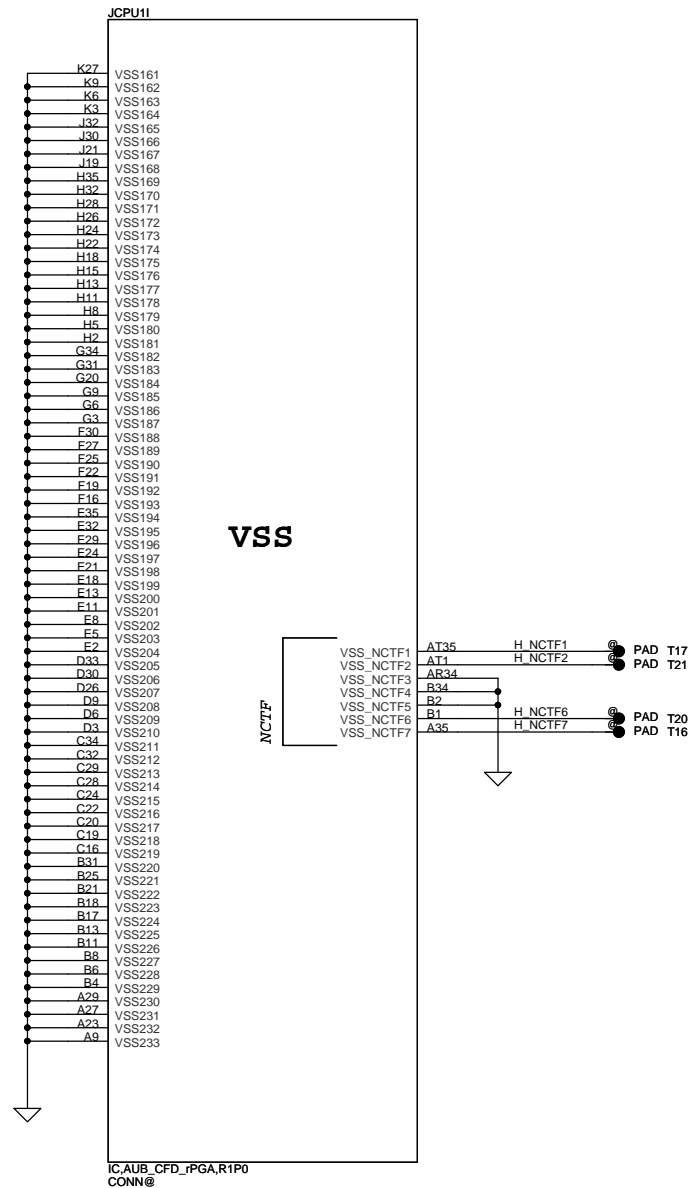
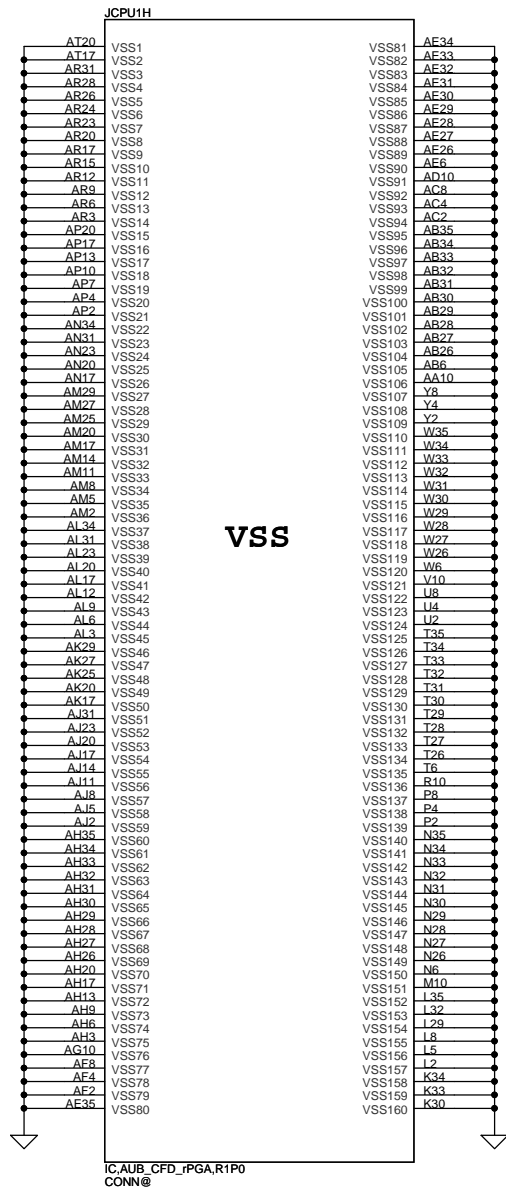


SENSE LINES
GRAPHICS VIDS
3A
DDR3 - 1.5V RAILS

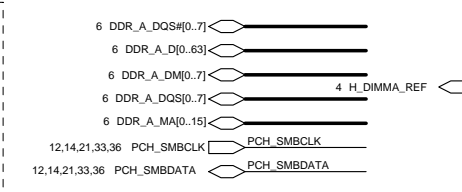
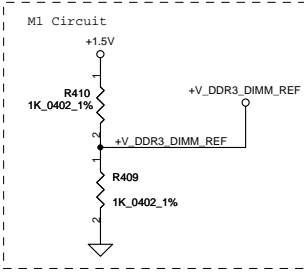
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1.8V

0.6A

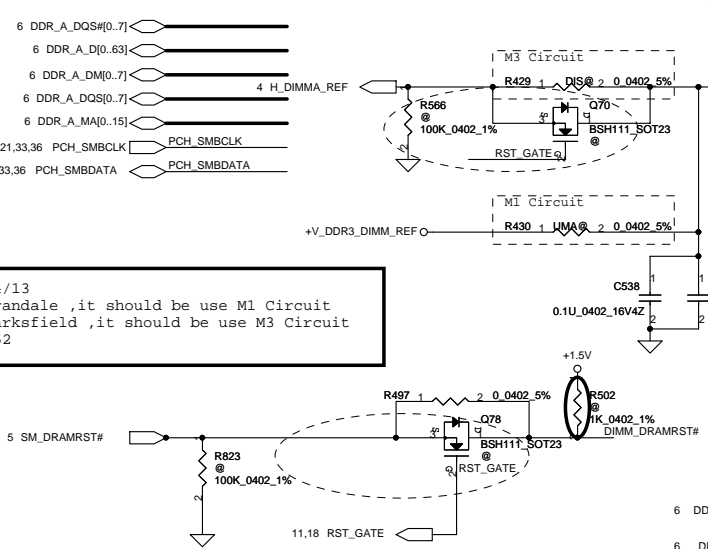
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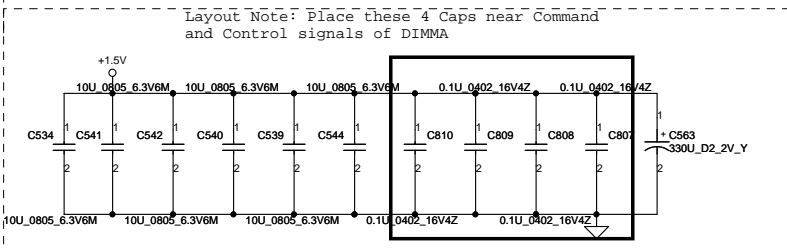
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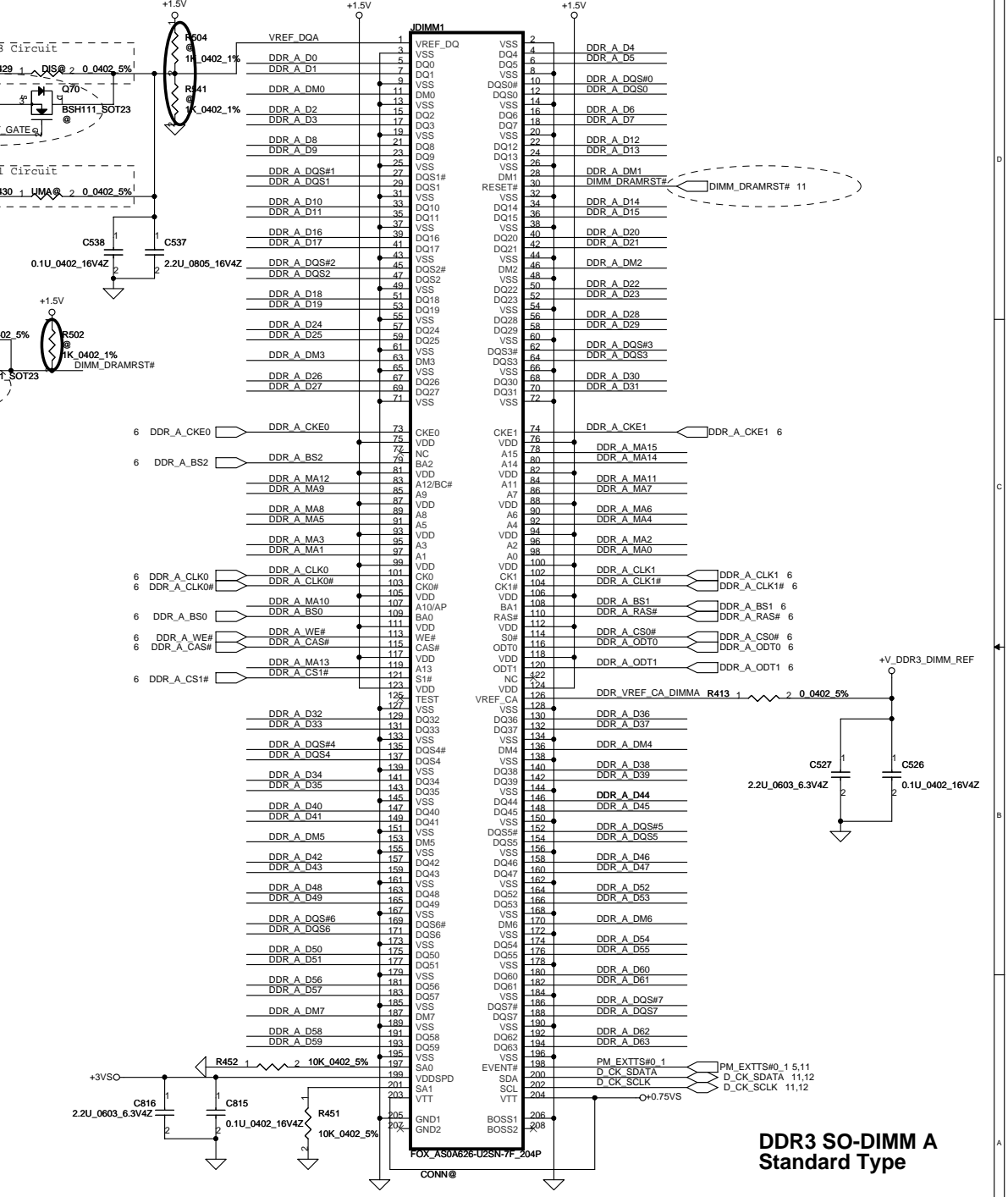
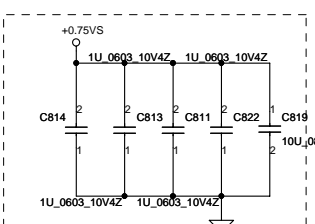
2009/04/13
For Arrandale ,it should be use M1 Circuit
For Clarkfield ,it should be use M3 Circuit
DG V1.52



Layout Note:
Place near JDIMM1

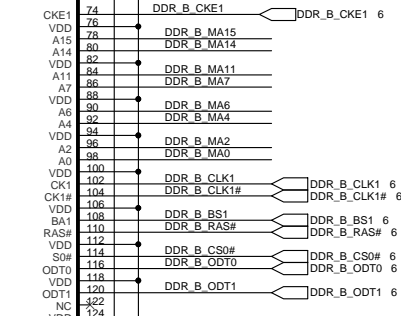
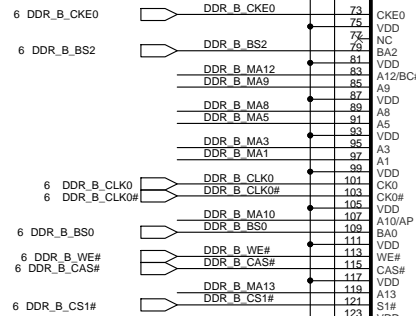
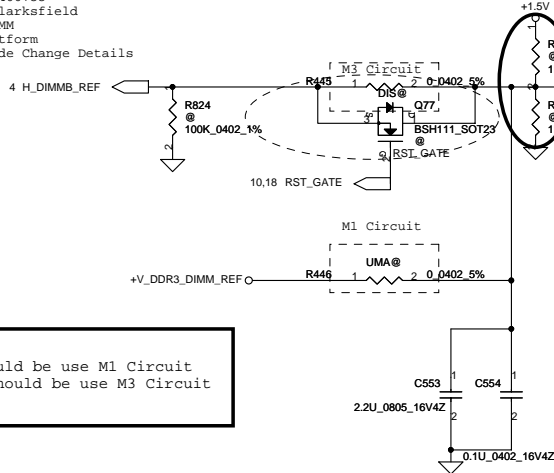


Layout Note:
Place near JDIMM1.203 & JDIMM1.204

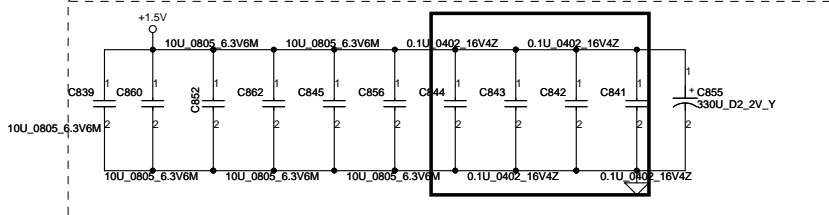
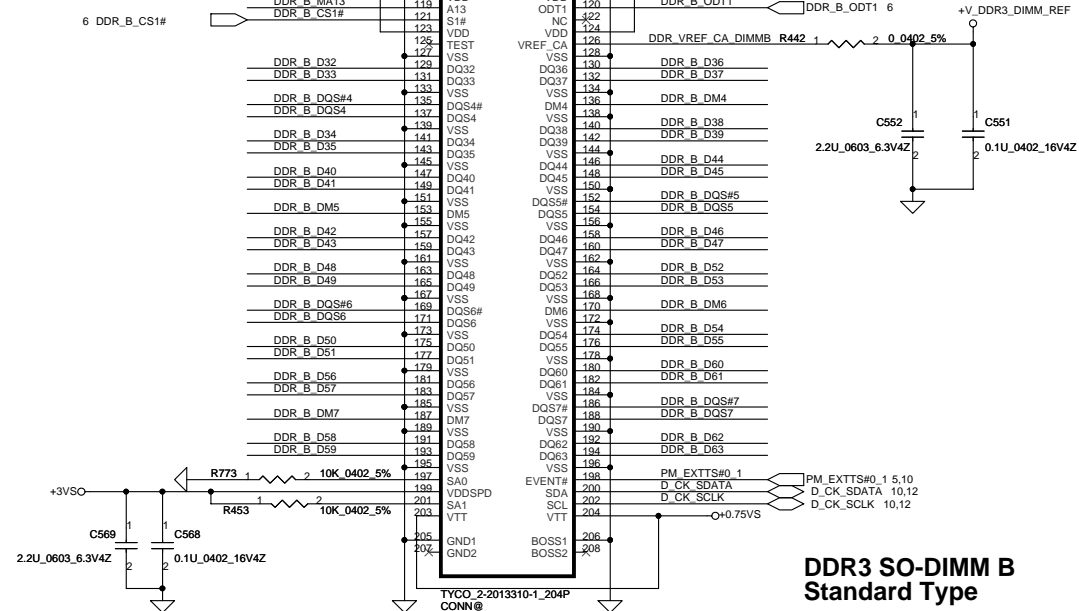


DDR3 SO-DIMM A
Standard Type

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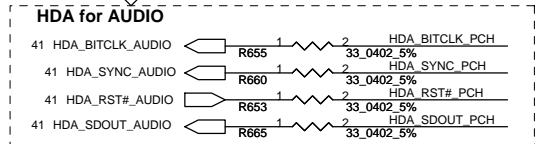
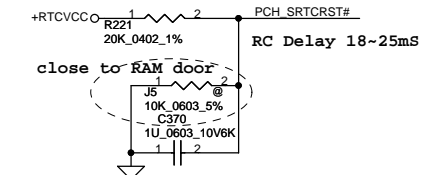
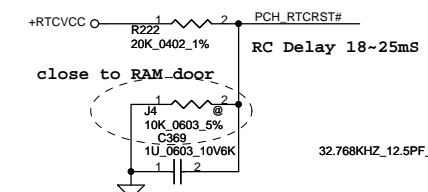


Layout Note: Place these 4 Caps near Command and Control signals of DIMMA

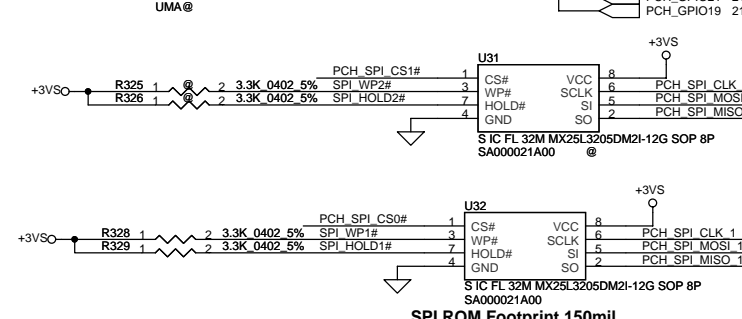
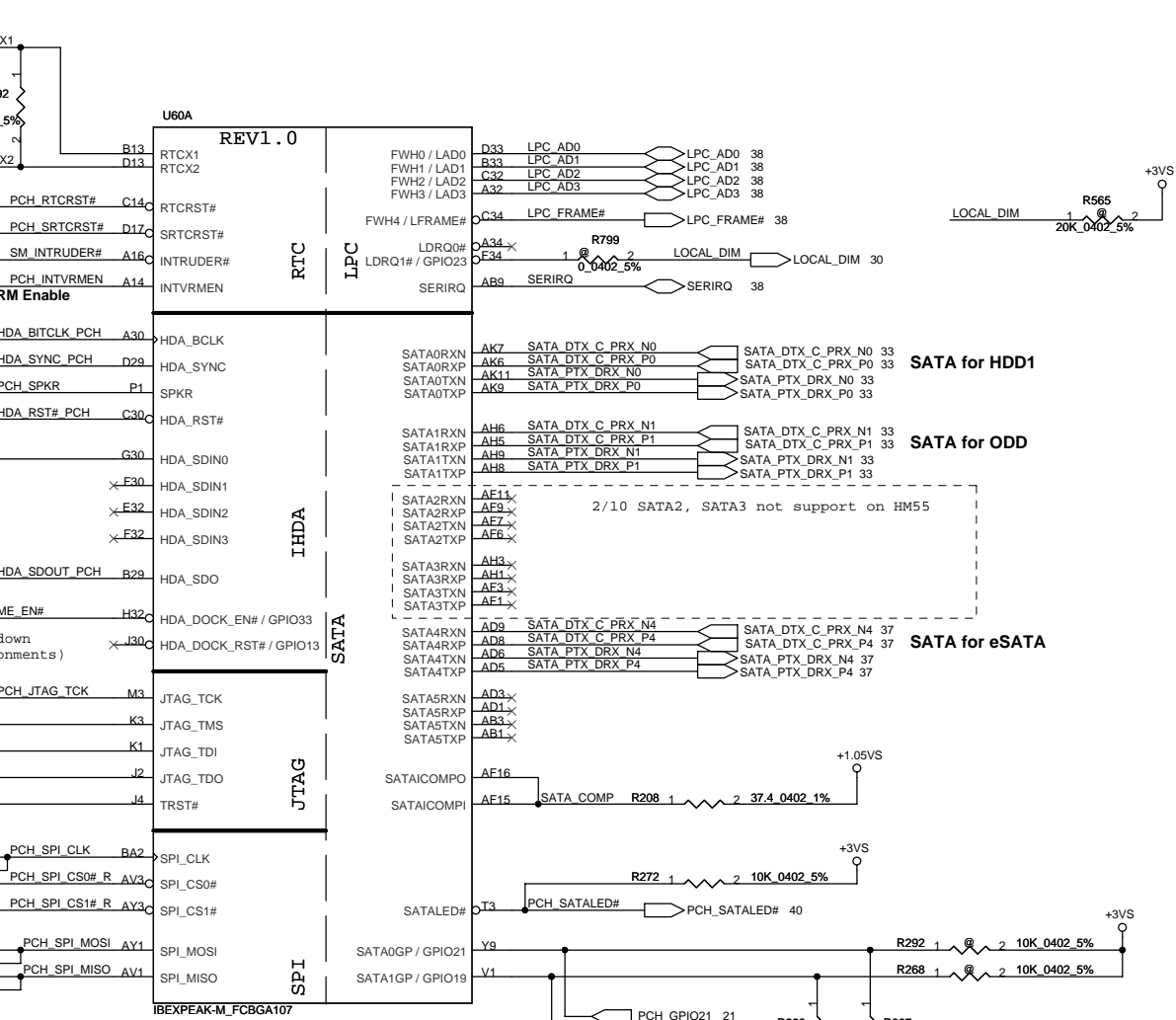
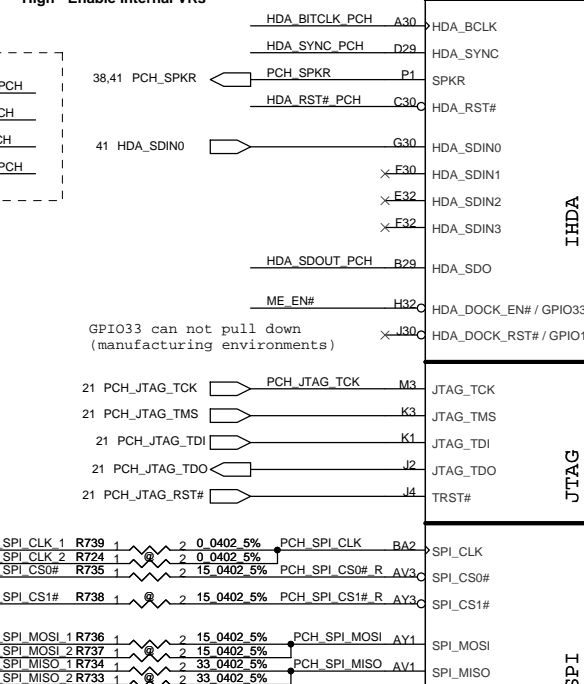
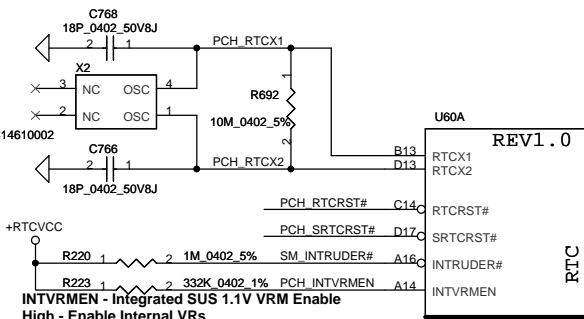
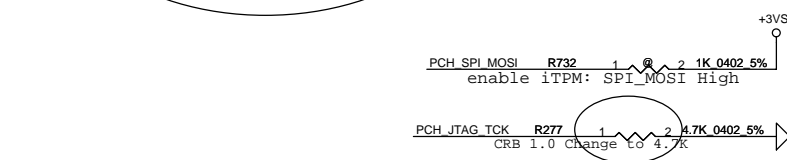
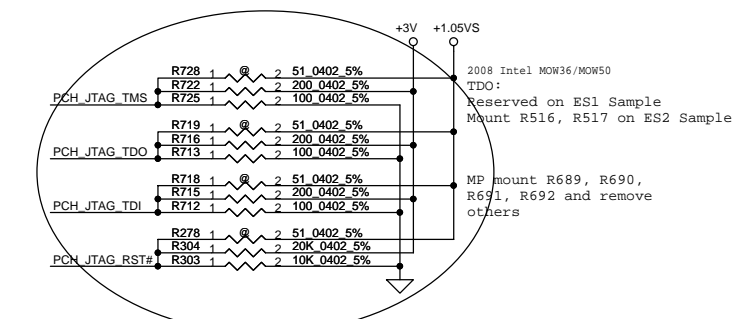
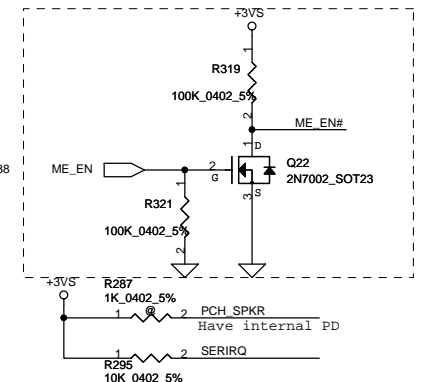
[illegible]

DDR3 SO-DIMM B Standard Type

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If GPIO33 pull down, ME will not working.
For factory update ME, pull down resistor pull under door.



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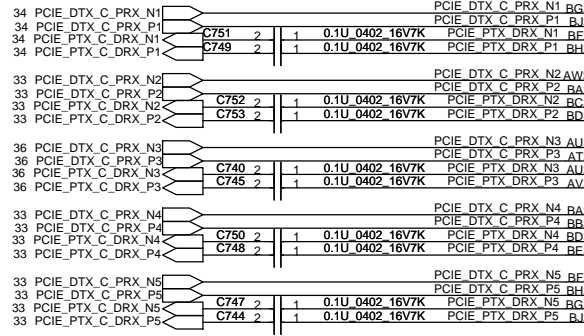
For PCIE LAN

For Wireless LAN

For NEWCRAD

For Mini2

For CardReader



2/10 PCIE7, PCIE8 not support on HM55

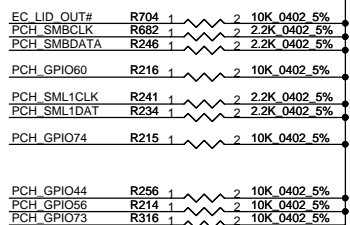
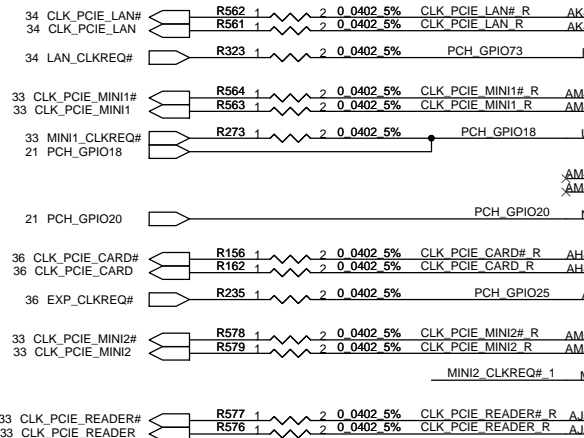
For PCIE LAN

For Wireless LAN

For NEWCRAD

For Mini2

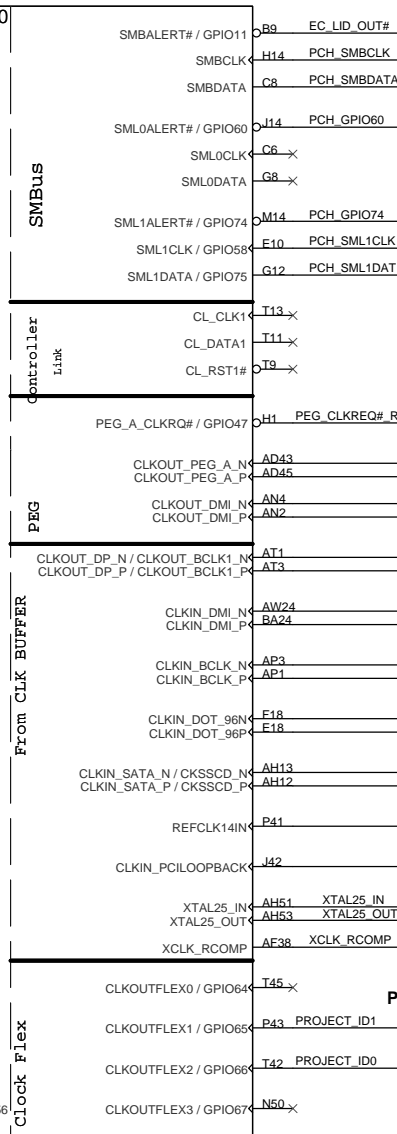
For CardReader



U60B

REV1.0

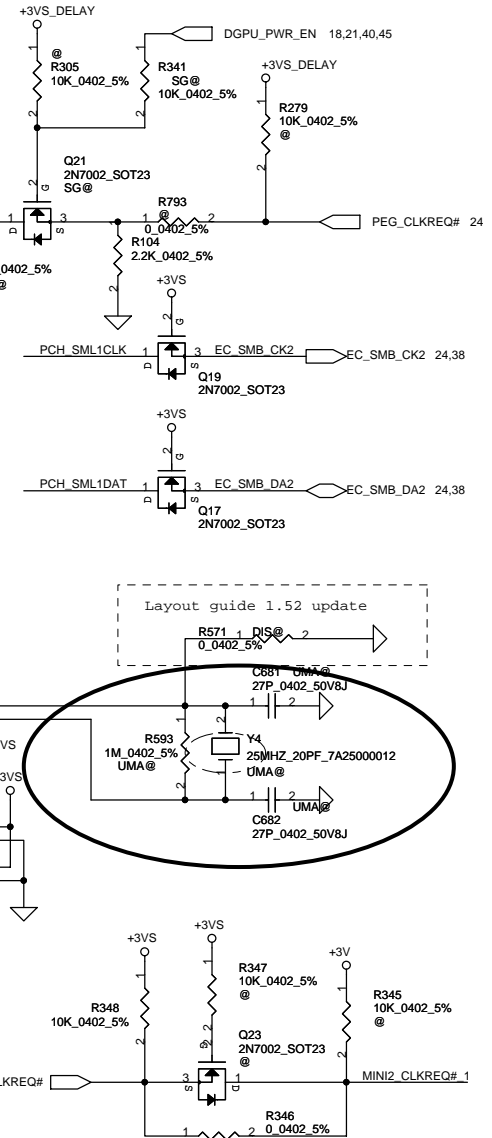
PCI-E*



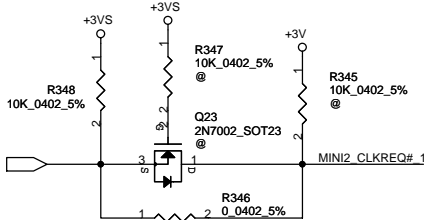
Project Port ID

Project ID		
ID1	ID0	Project
0	0	JV
0	1	Future

1. Connect Directly EXPRESS CARD, MINI1, MINI2
2. Level Shift1, Pull-Up to +3VS CLOCK GEN, DIMM1, DIMM2
3. Level Shift2, Pull-Up to +3VS LAN
4. Level Shift3, Pull-Up to +3VS CPU & PCH XDP

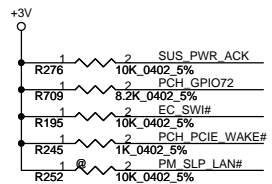
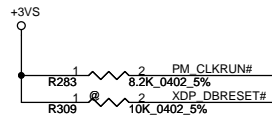
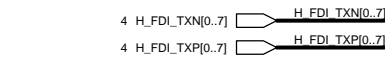
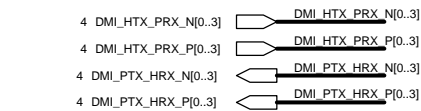


Layout guide 1.52 update

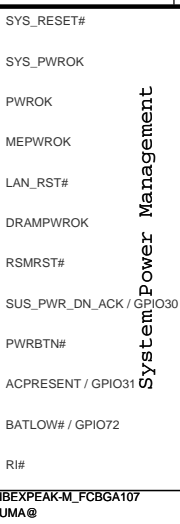
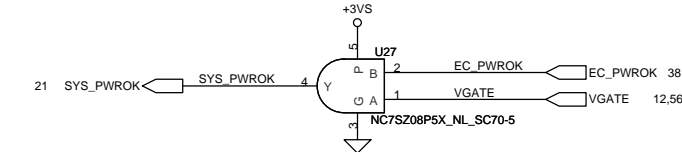
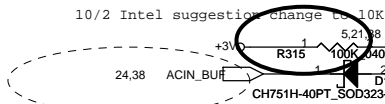
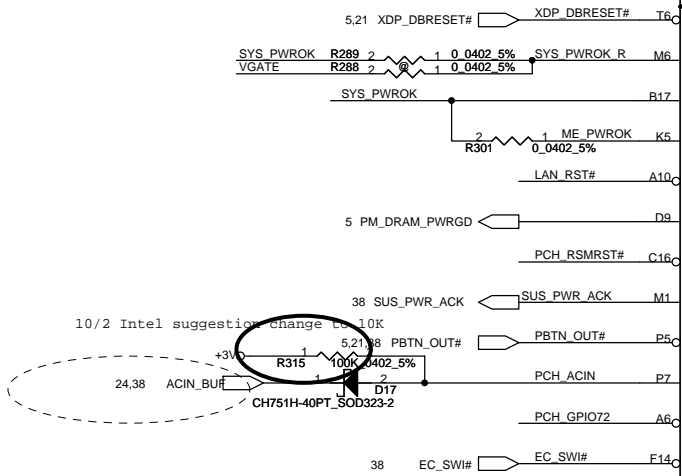
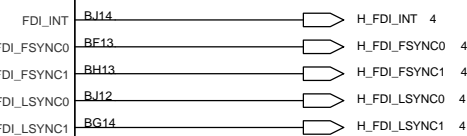
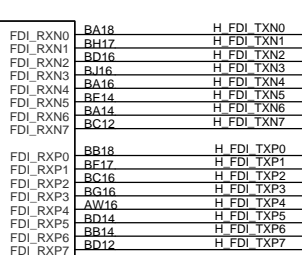
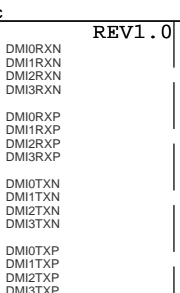
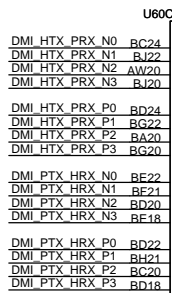
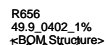


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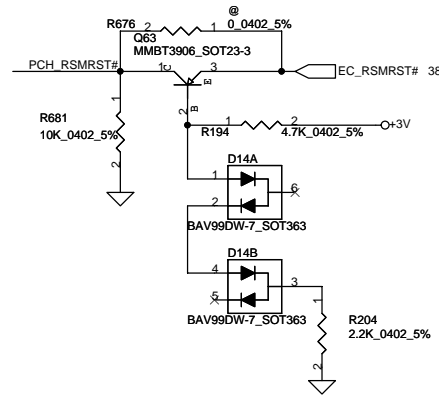
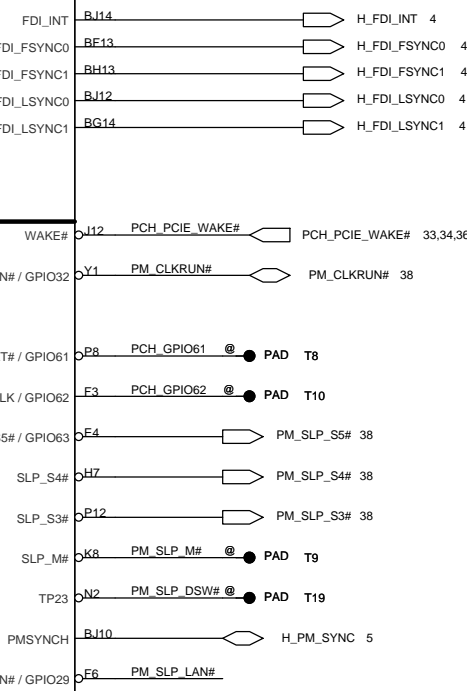
WWW.AliSaler.Com



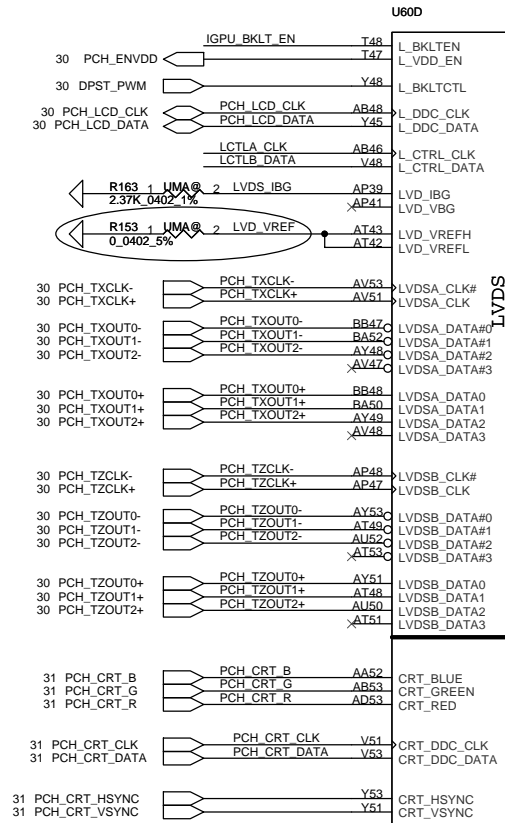
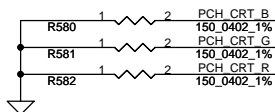
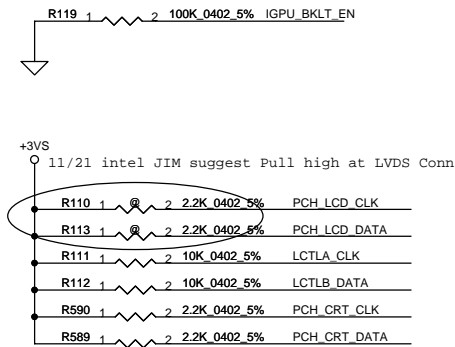
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System Power Management

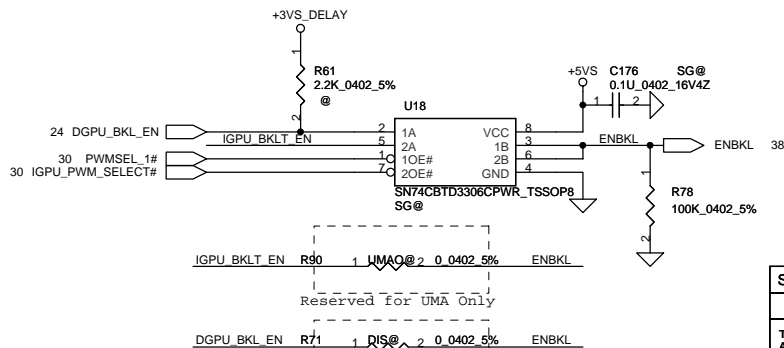
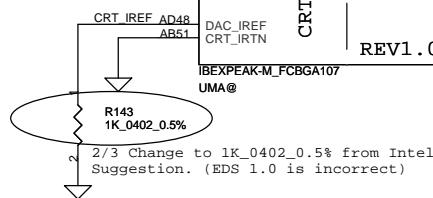


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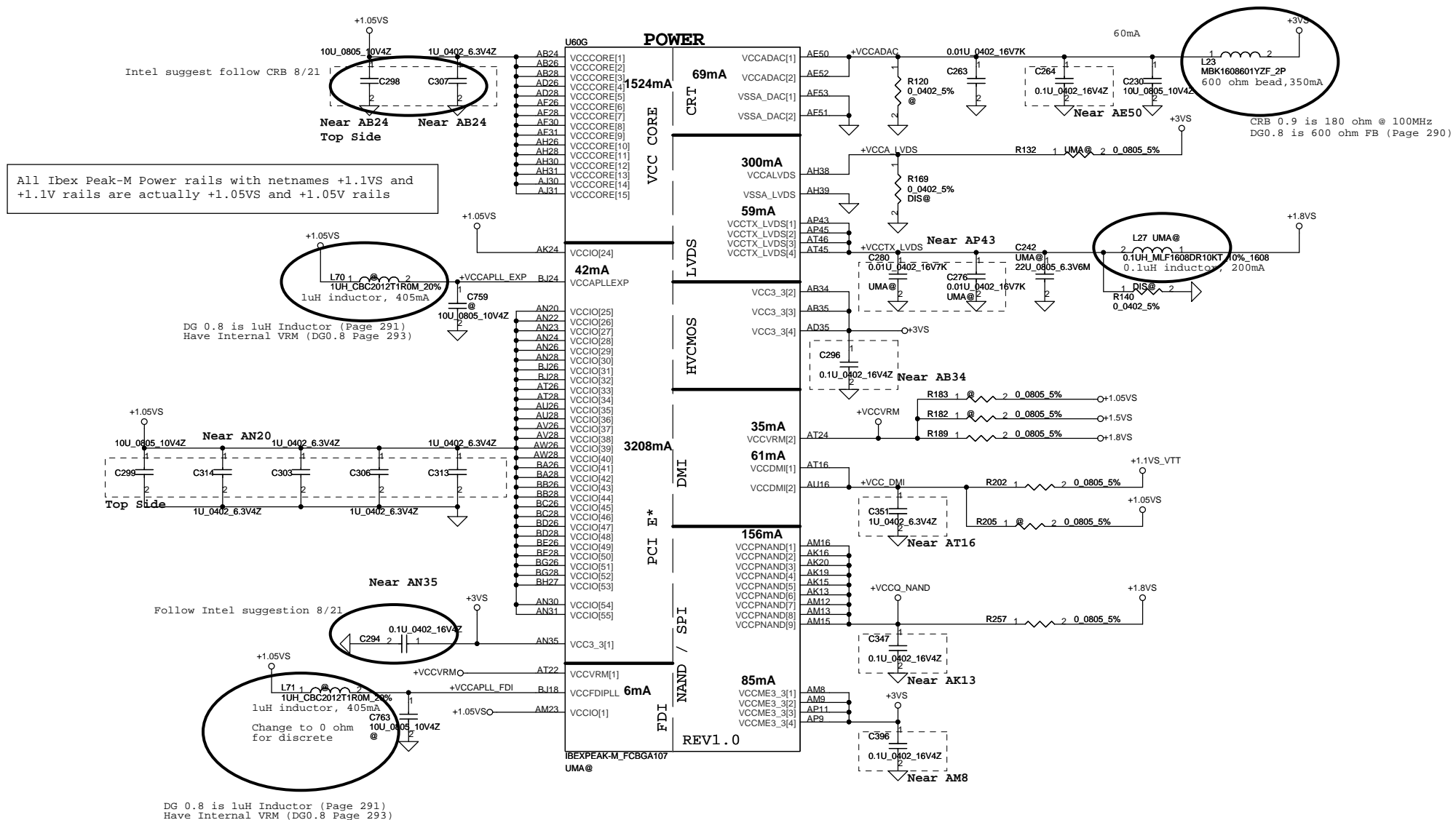


Digital Display Interface

REV1.0

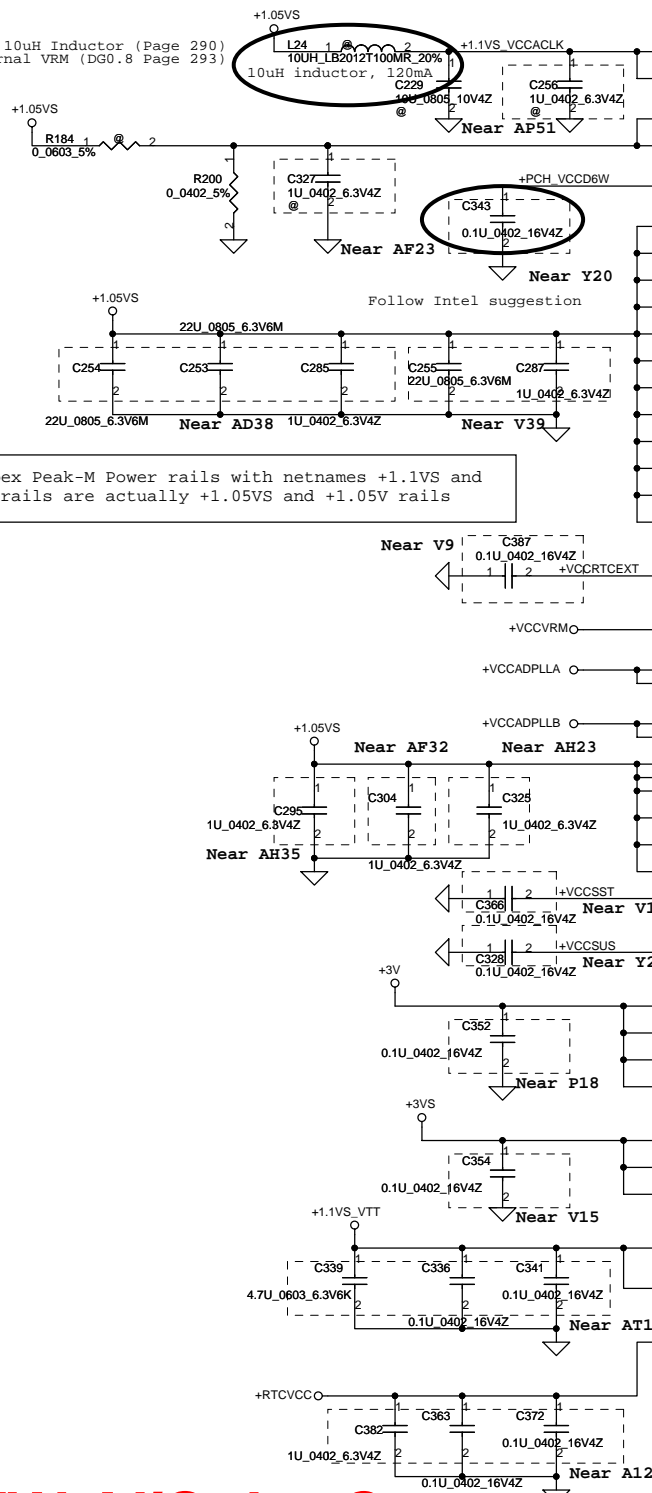


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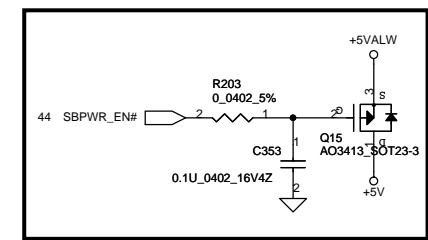
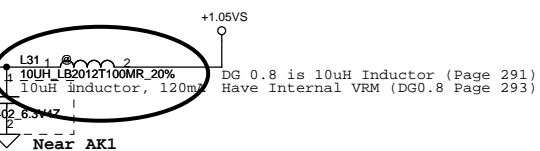
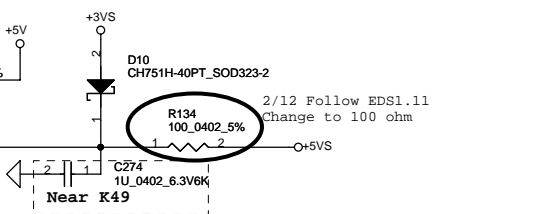
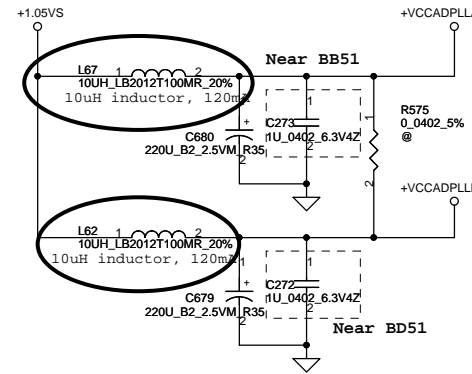
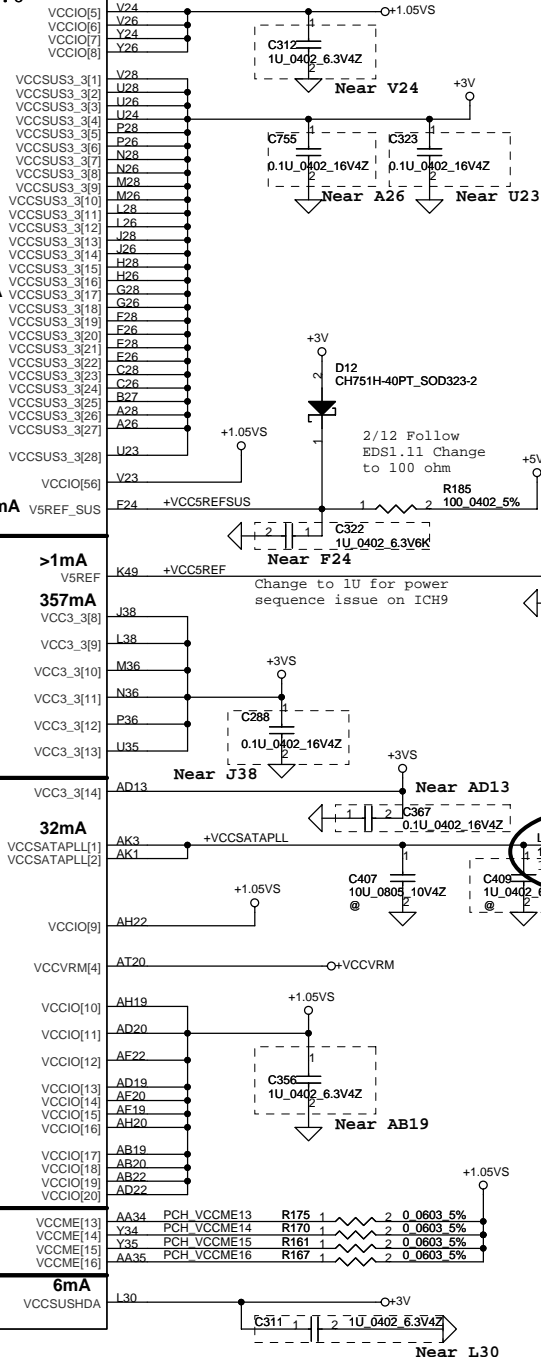
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DG 0.8 is 10uH Inductor (Page 290)
Have Internal VRM (DG0.8 Page 293)



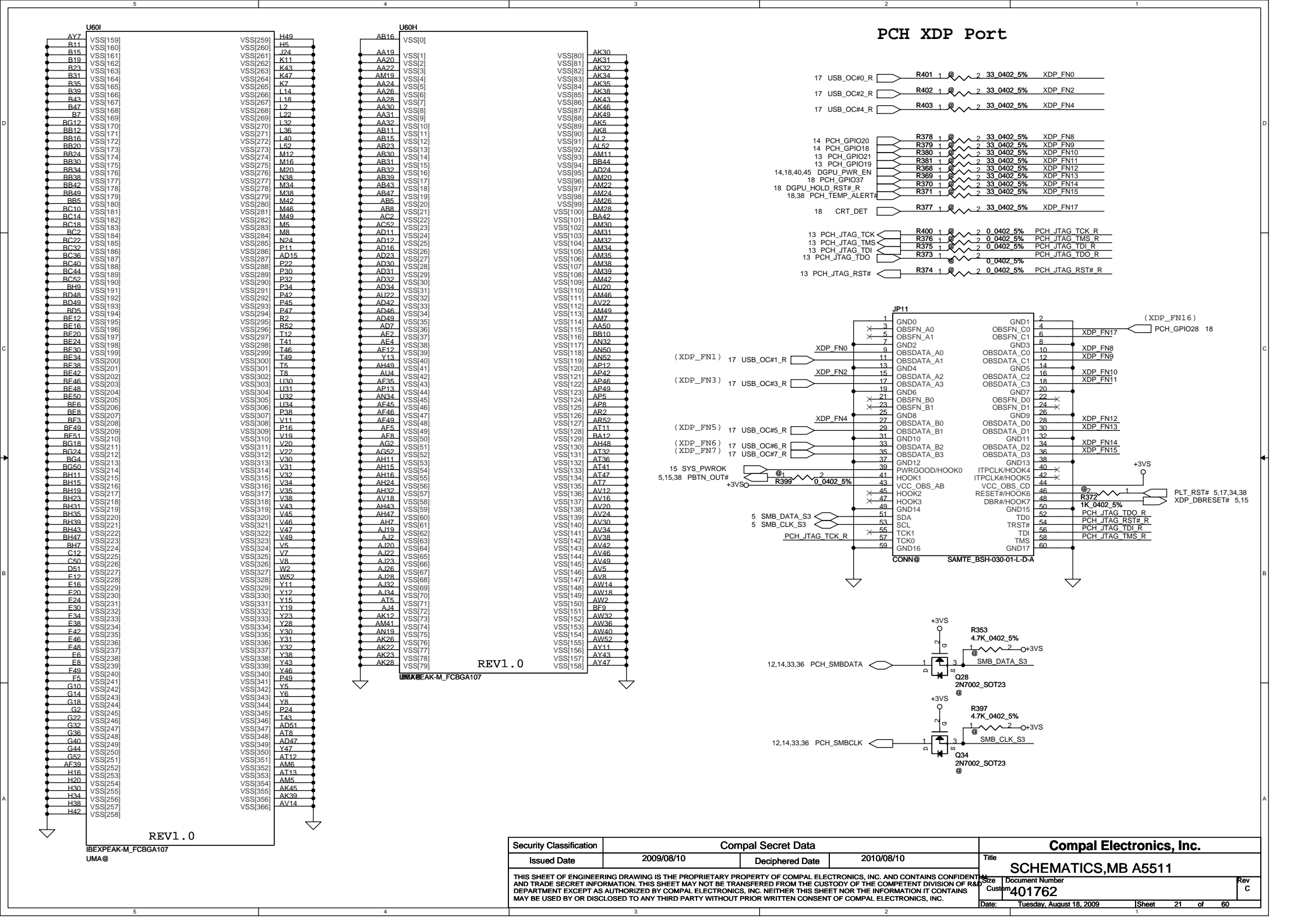
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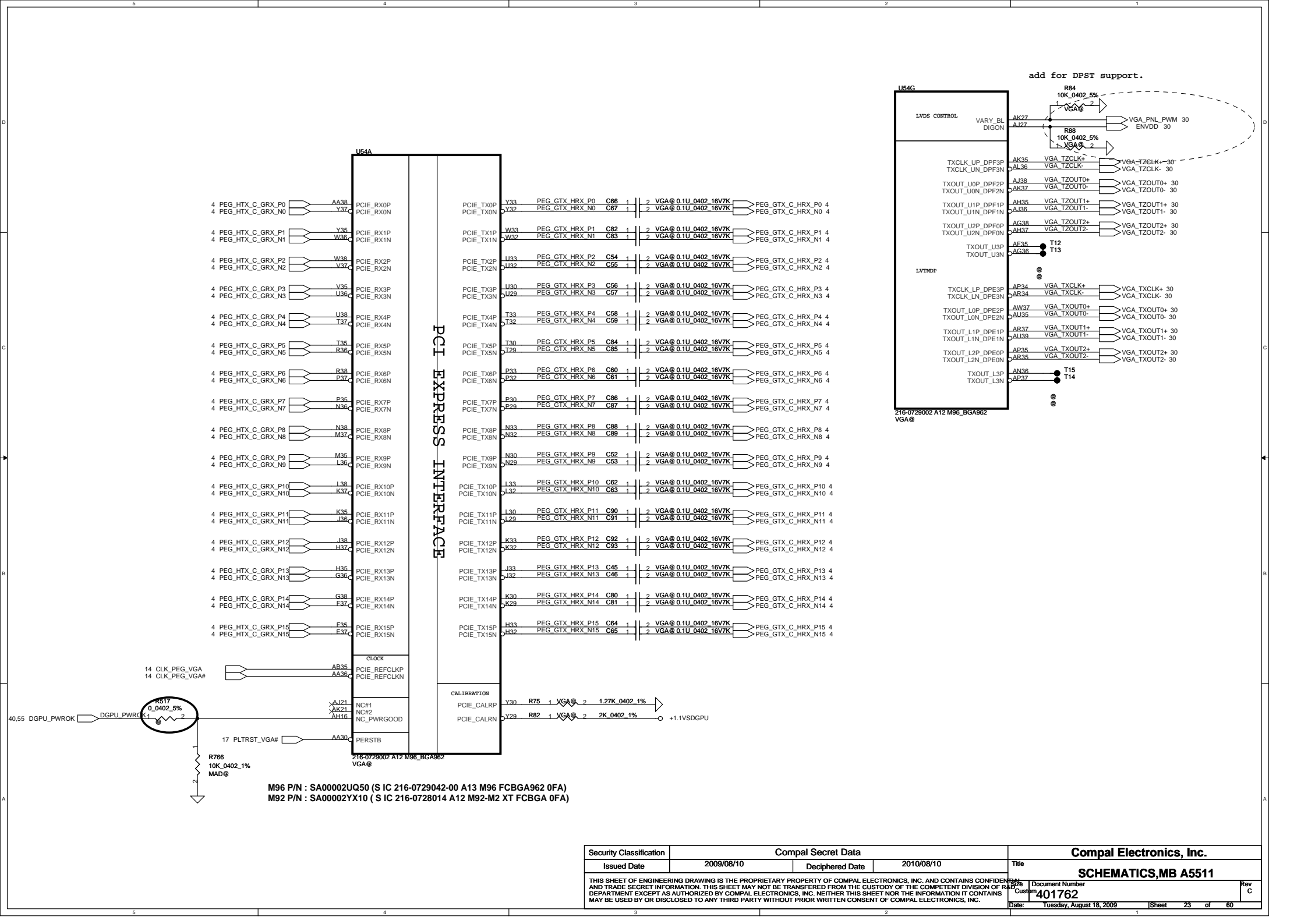
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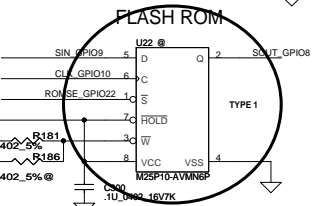
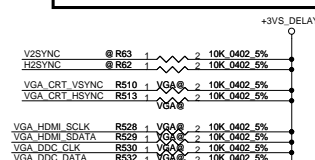
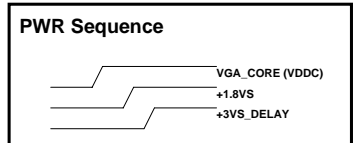
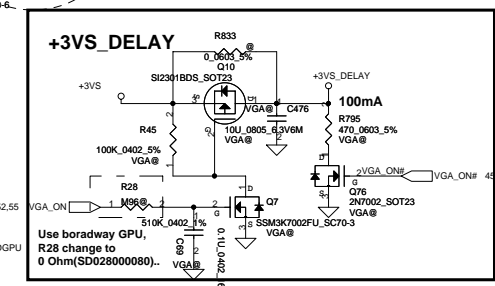
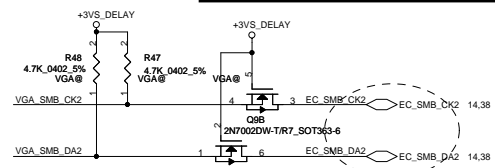
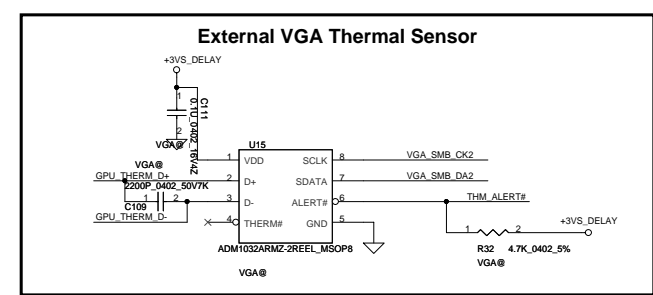
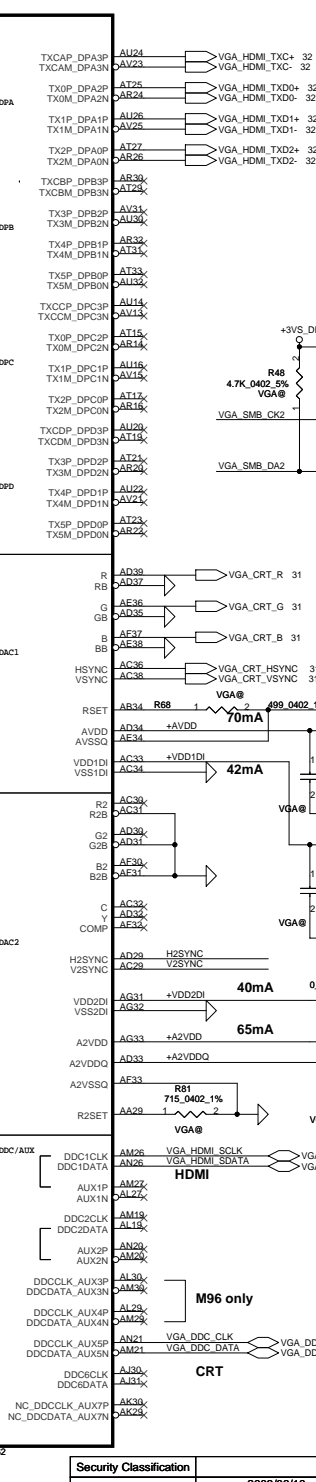
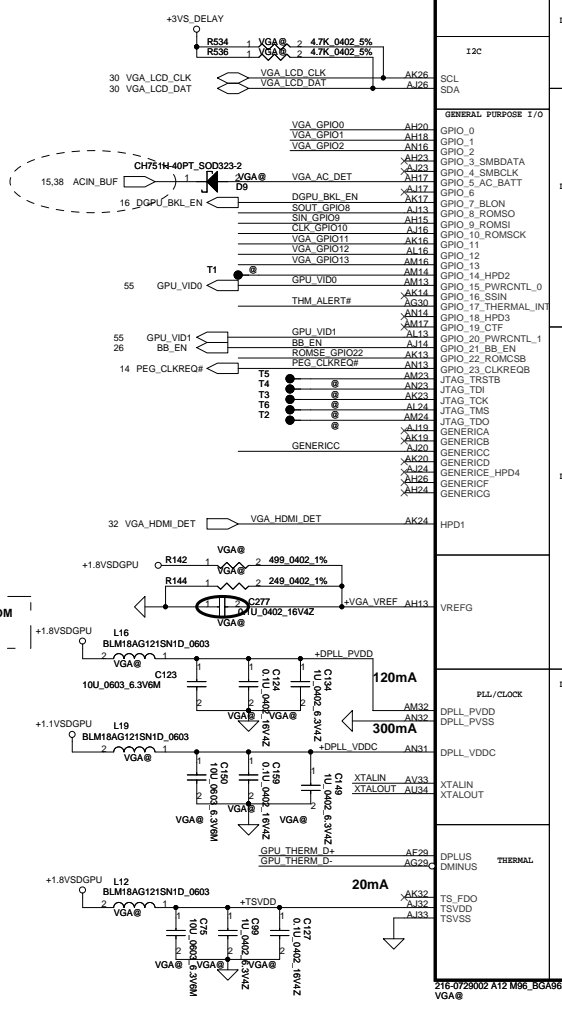
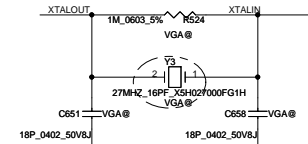
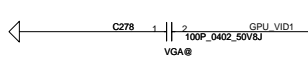
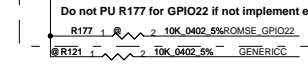
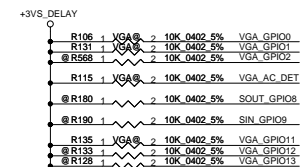
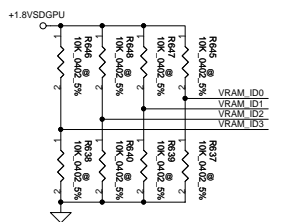
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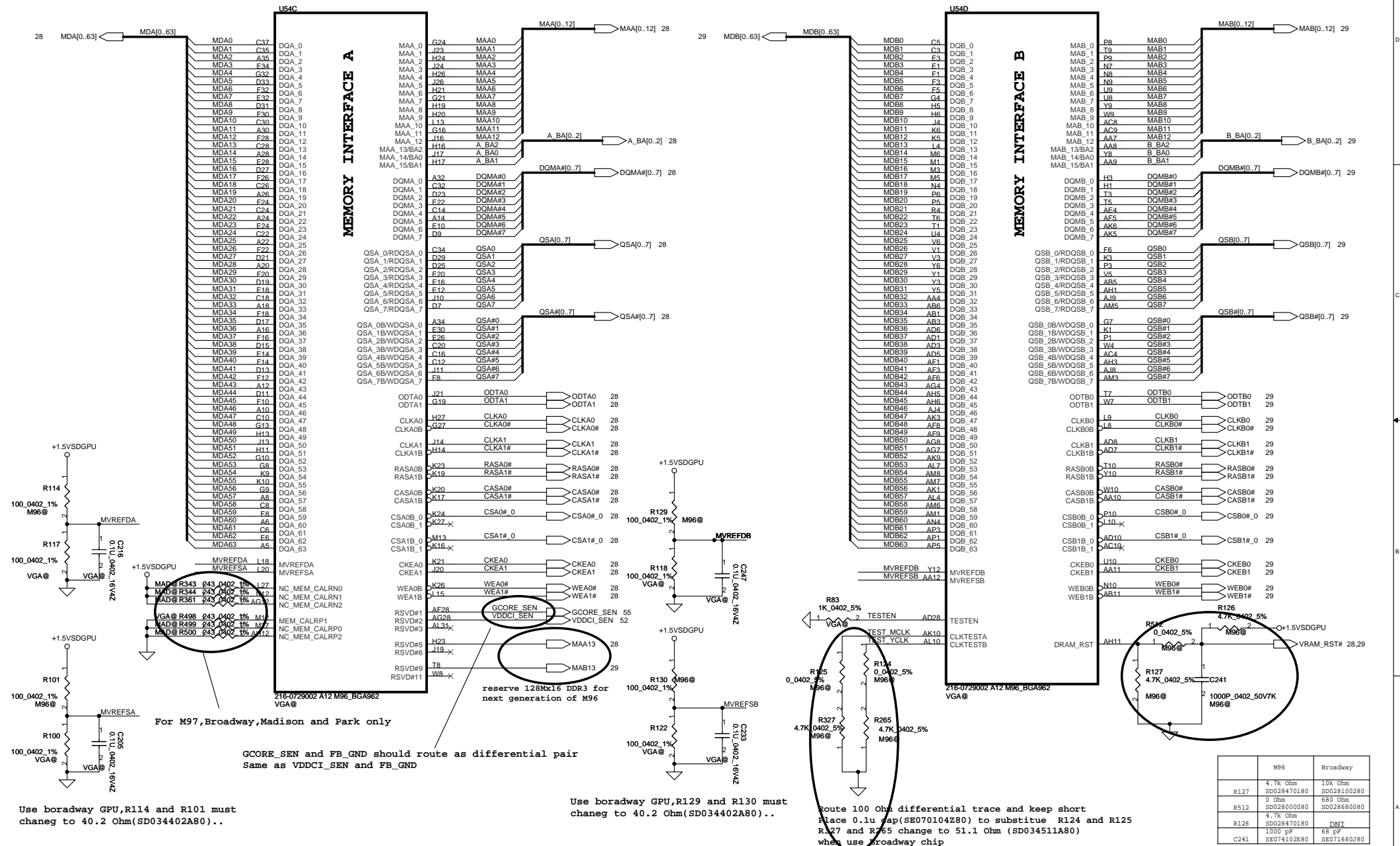




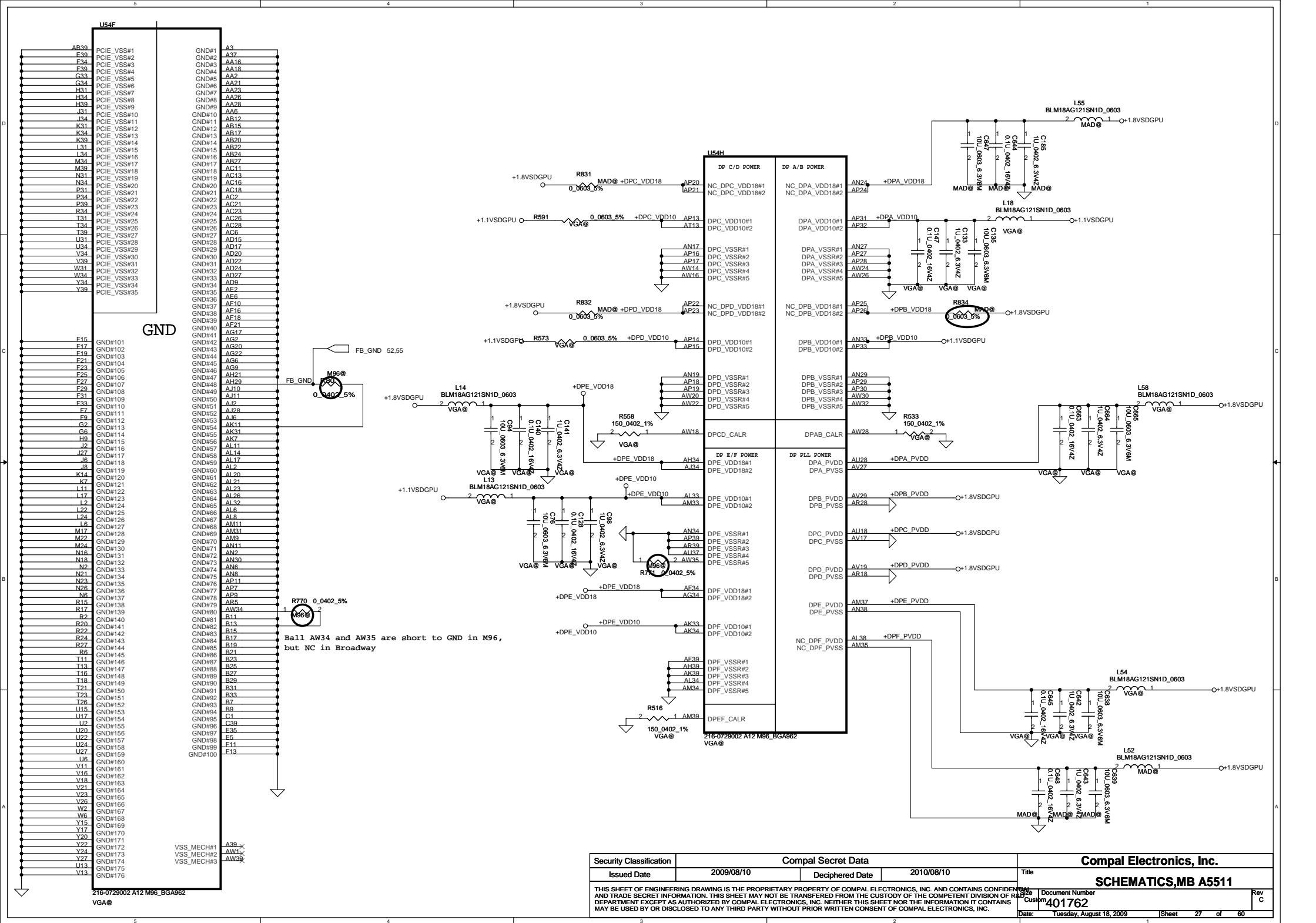
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HYNIX	1	0	0	0



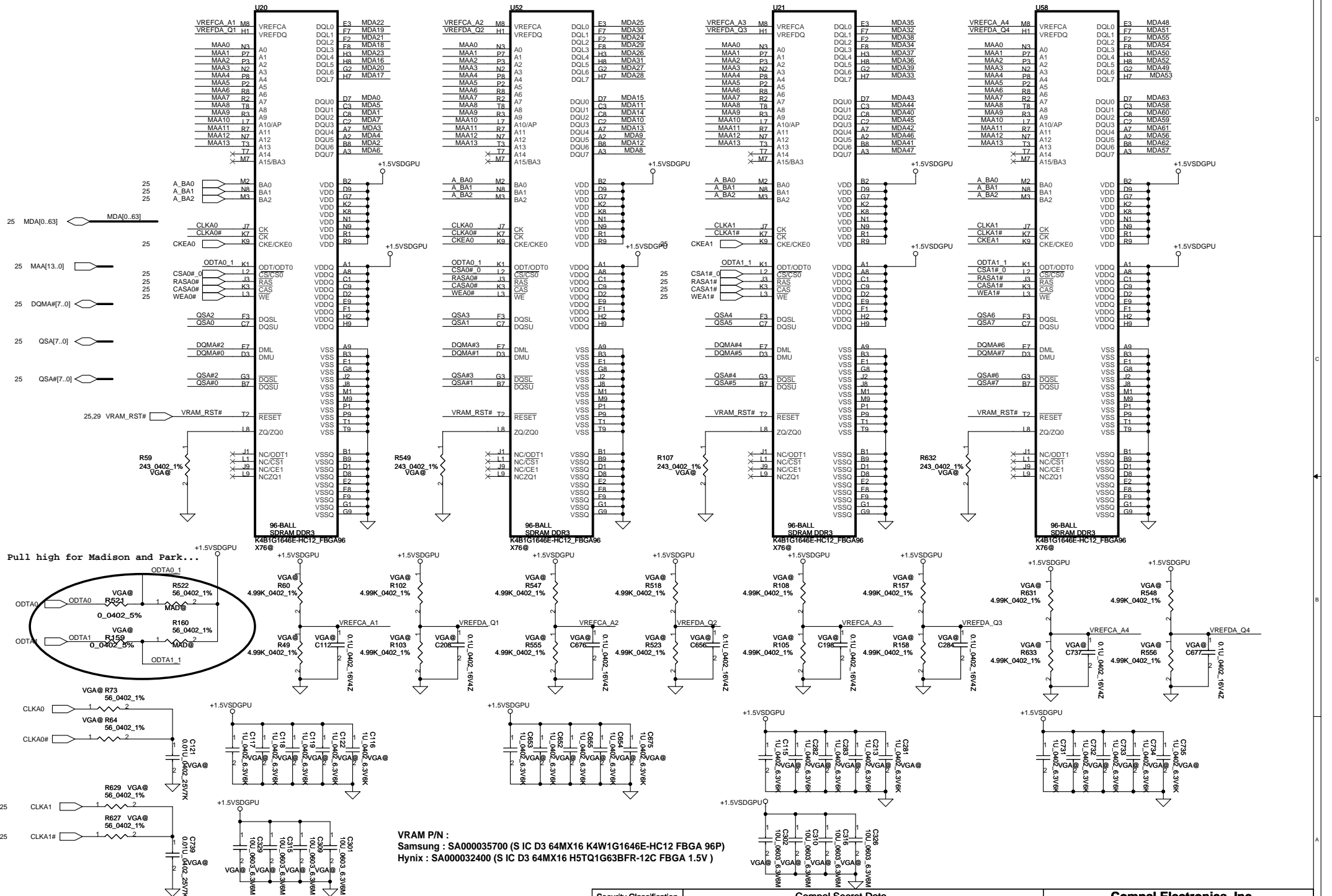
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Issued Date	2008/08/10	Deciphered Date	2010/08/10	Title	
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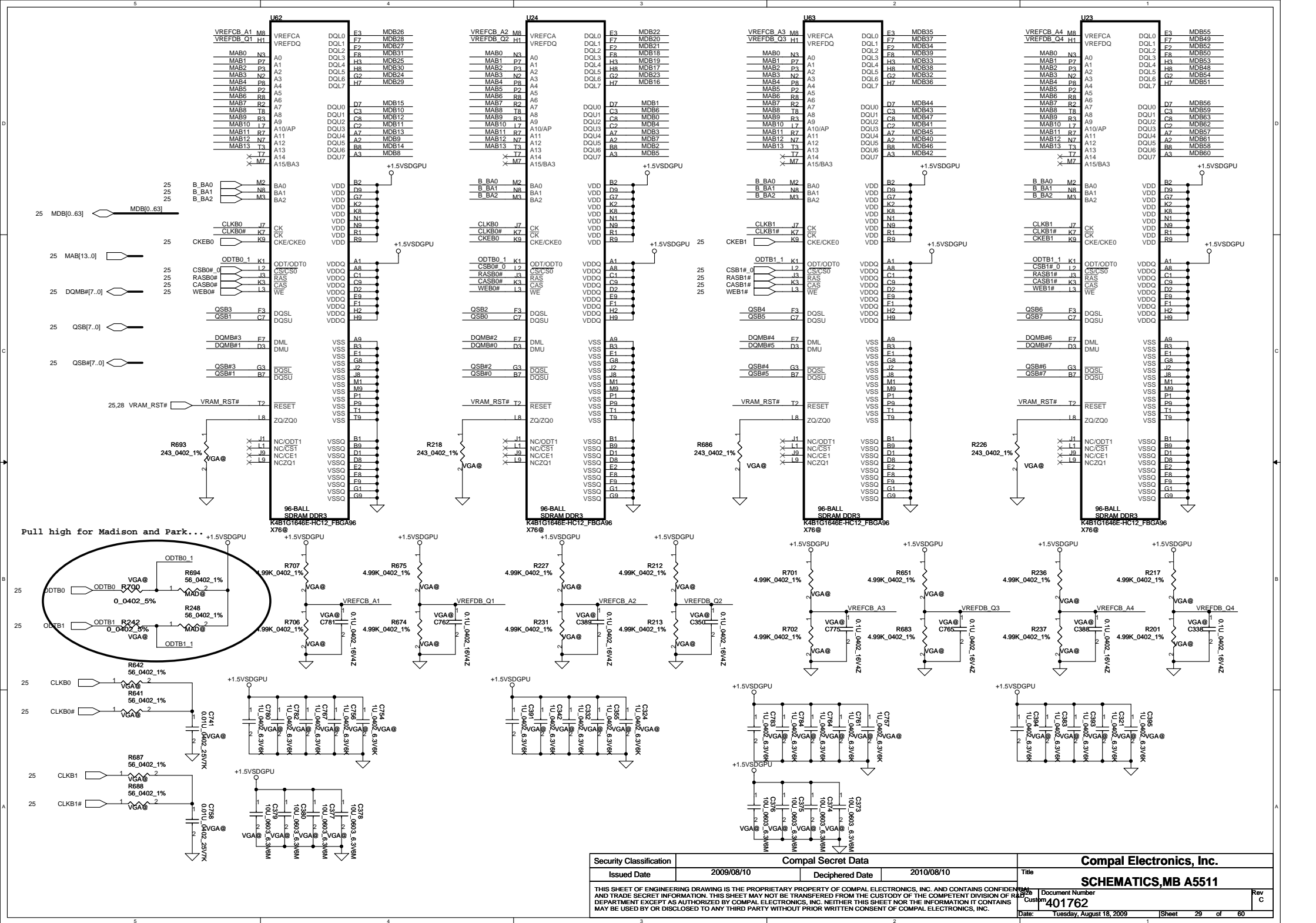
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Issued Date	2009/08/10	Deciphered Date	2010/08/10	Title
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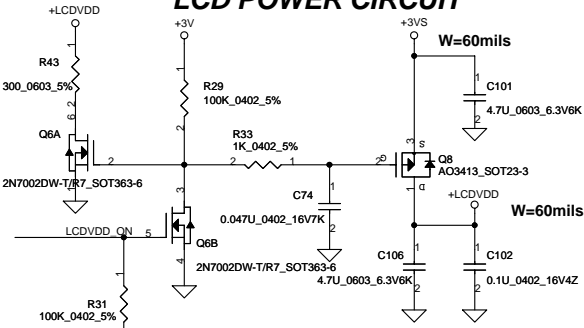
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Issued Date	2009/08/10	Deciphered Date	2010/08/10	Title
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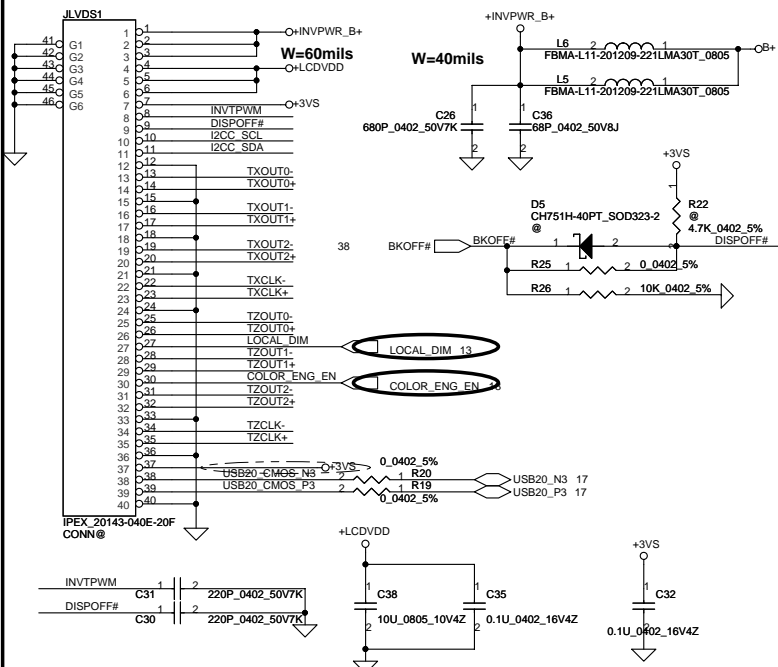
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						Customer		Document Number		Rev	
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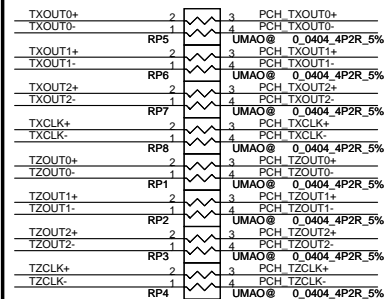
LCD POWER CIRCUIT



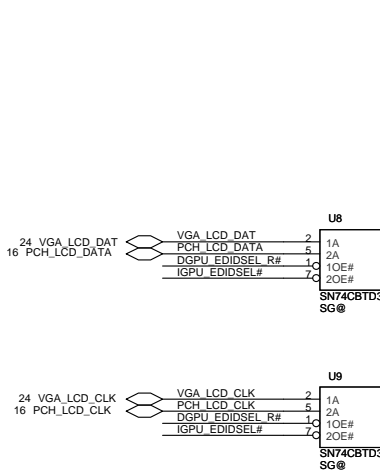
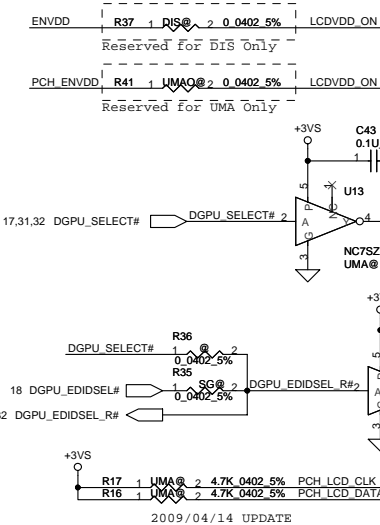
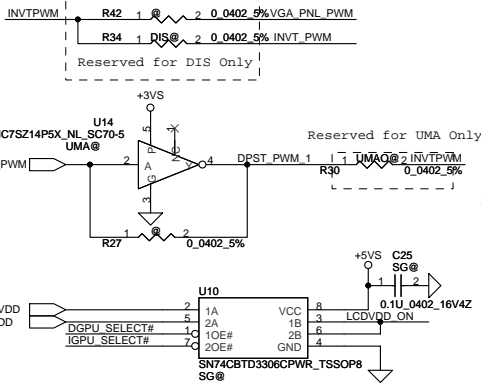
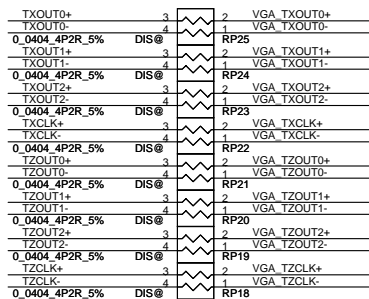
LED PANEL Conn.



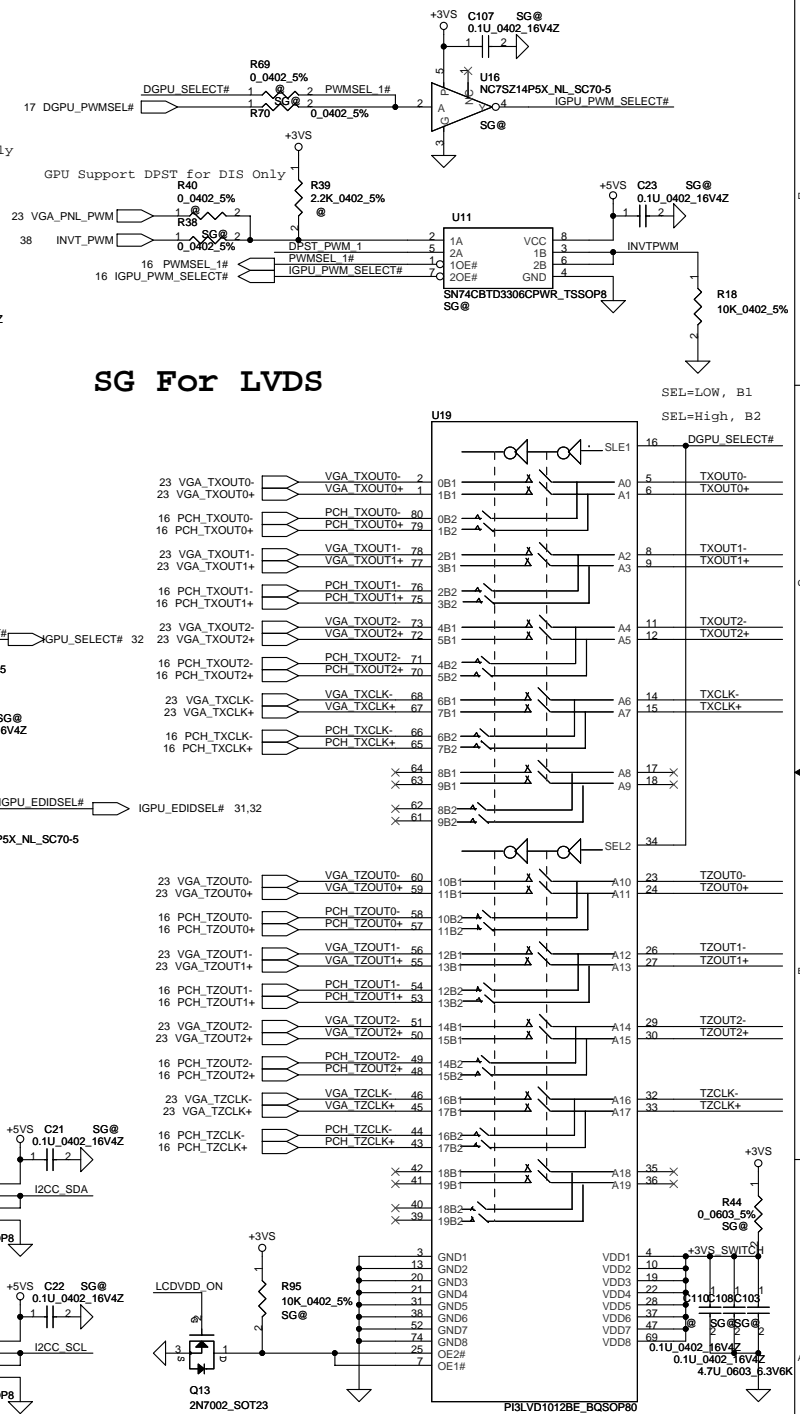
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DIS ONLY

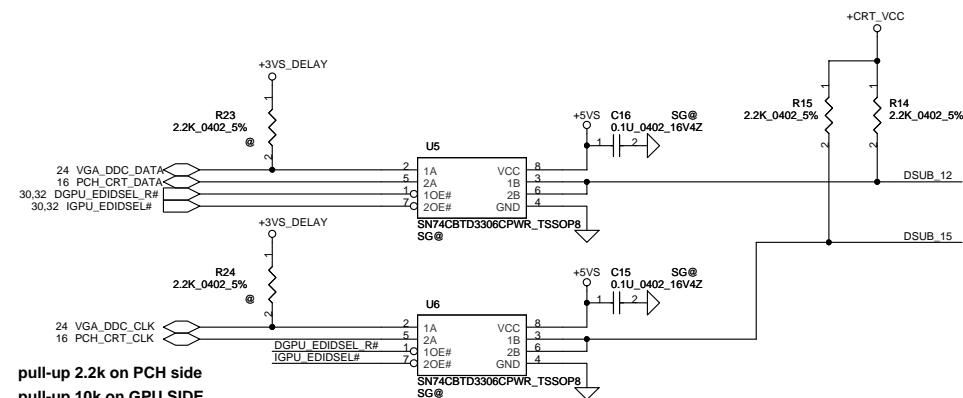
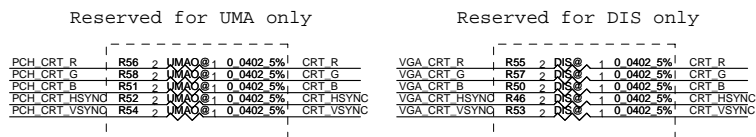
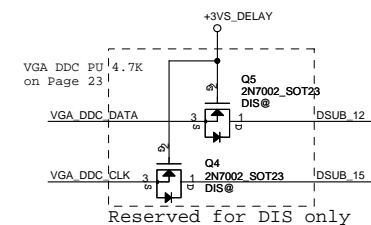
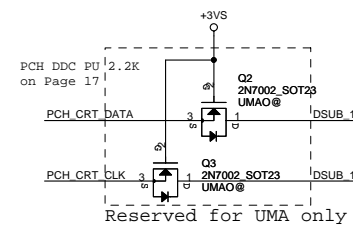
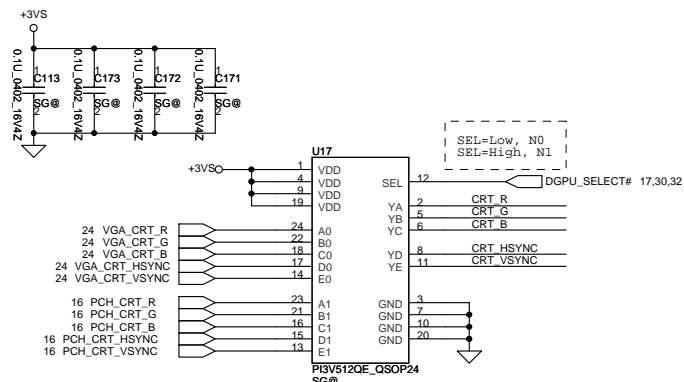
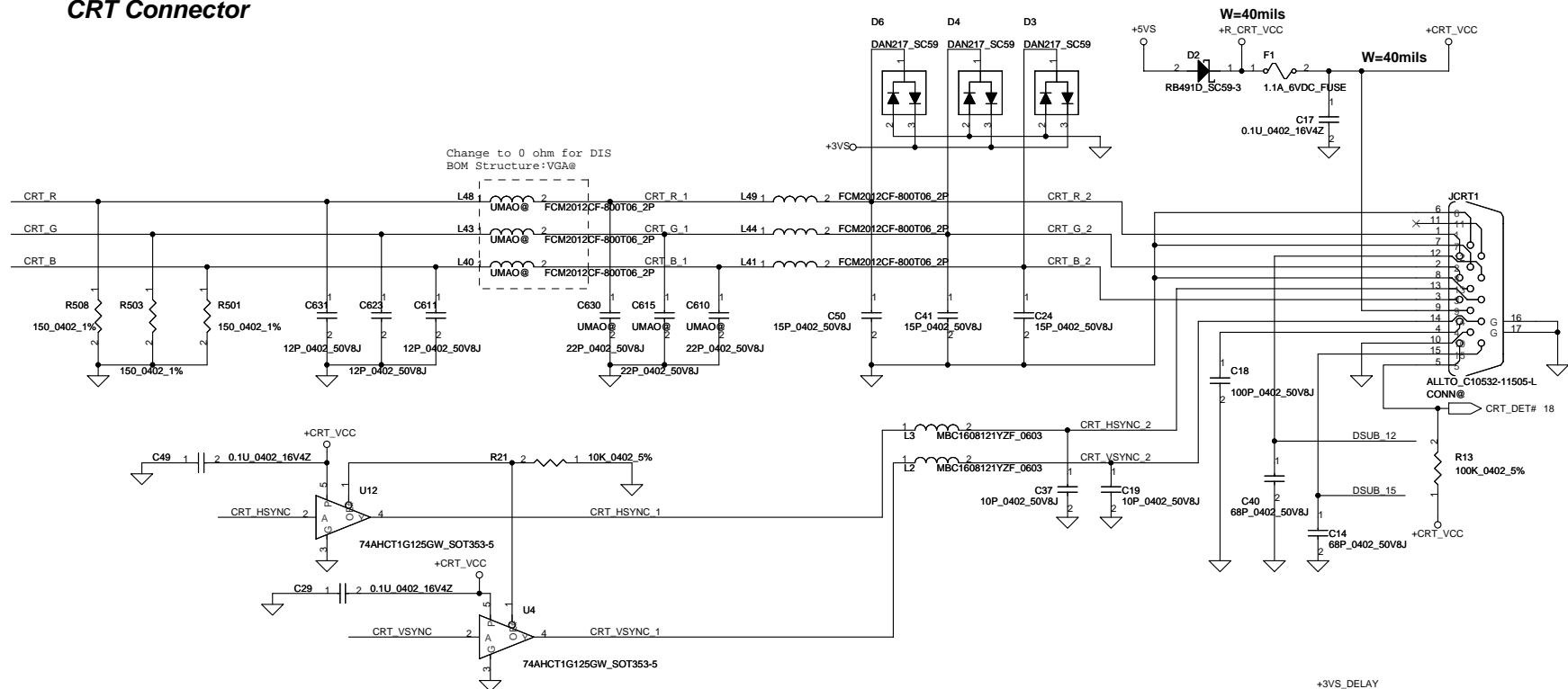


SG For LVDS



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CRT Connector



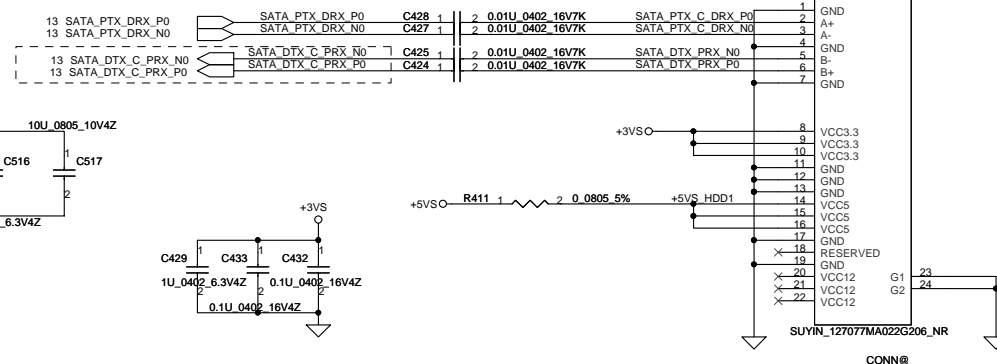
pull-up 2.2k on PCH side
pull-up 10k on GPU SIDE

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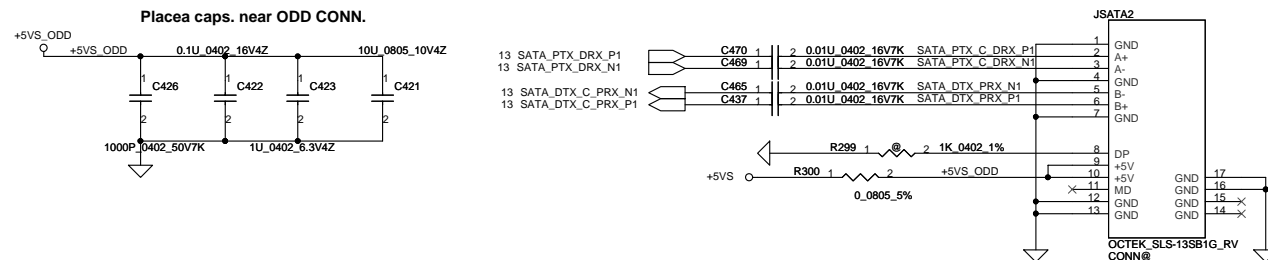
SATA HDD1 Conn.

CL 4.0 mm



SATA ODD Conn.

CL 6.0 mm



Card Reader & MINI CARD x2(WLAN & TV)

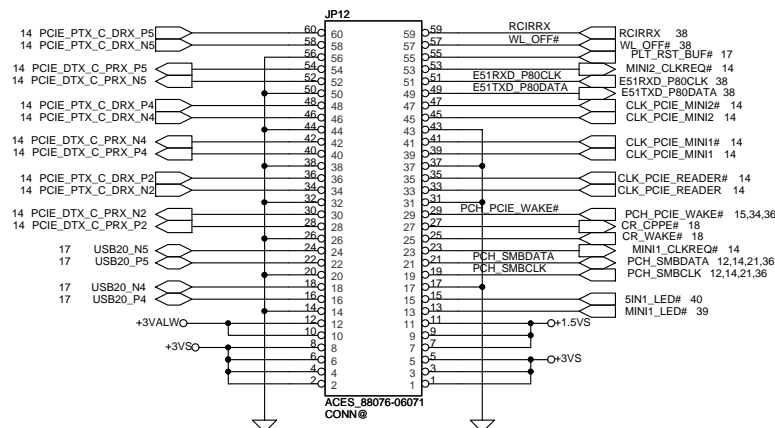
Card Reader

TV

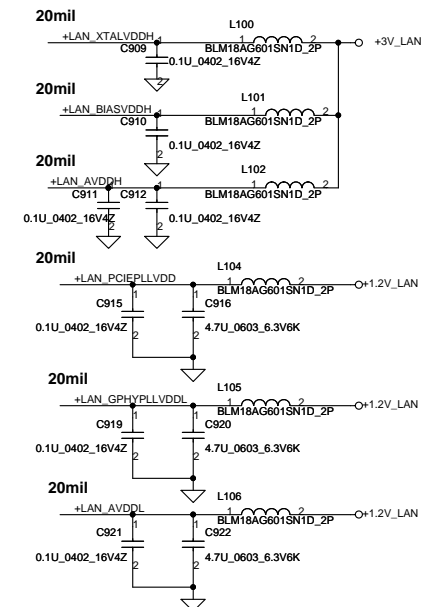
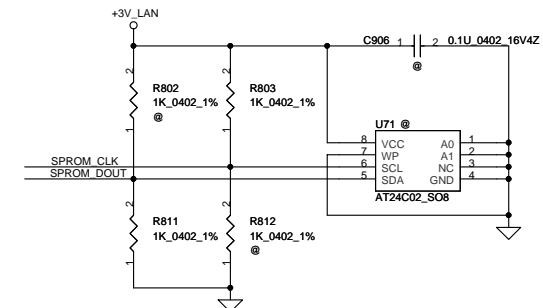
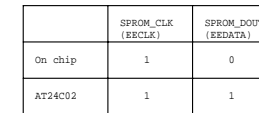
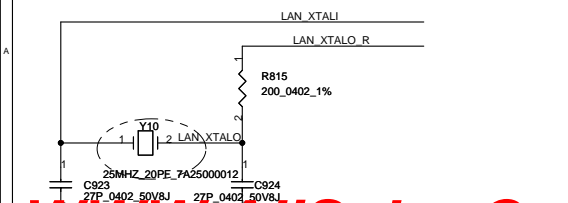
WLAN

TV

WLAN

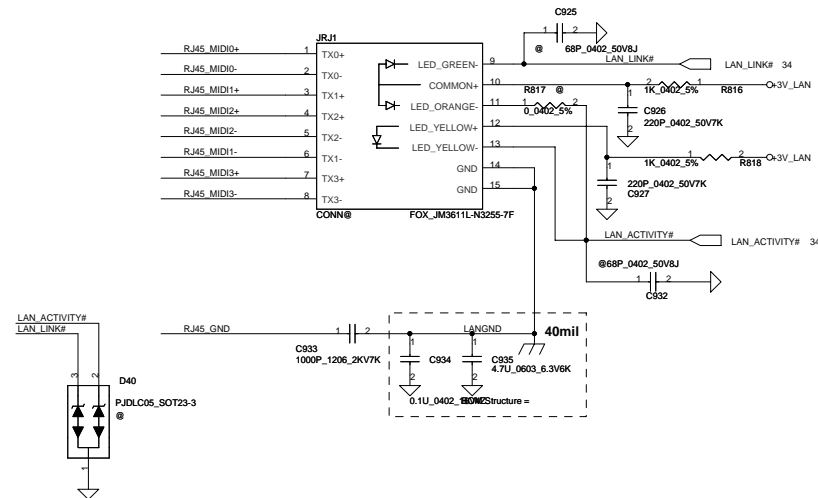
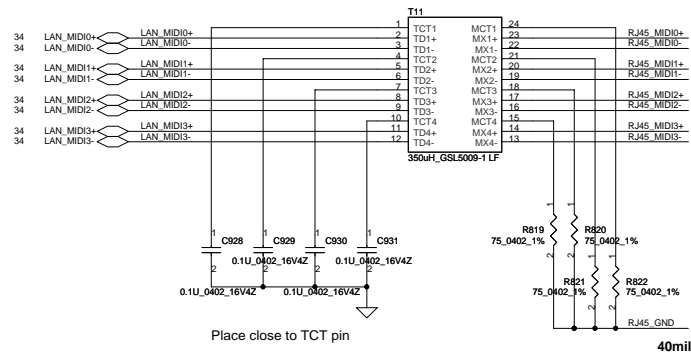


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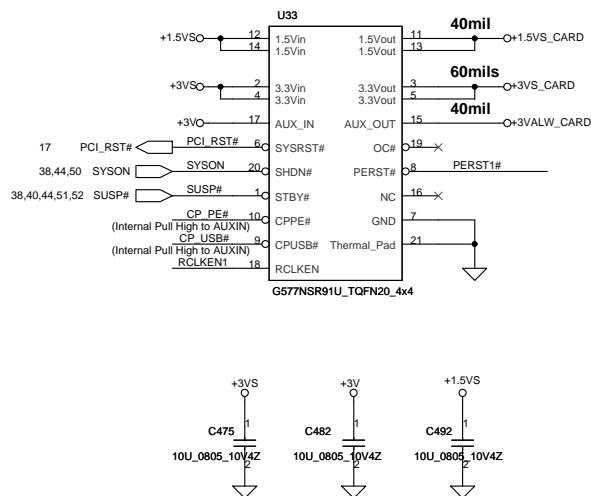
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LAN Connector

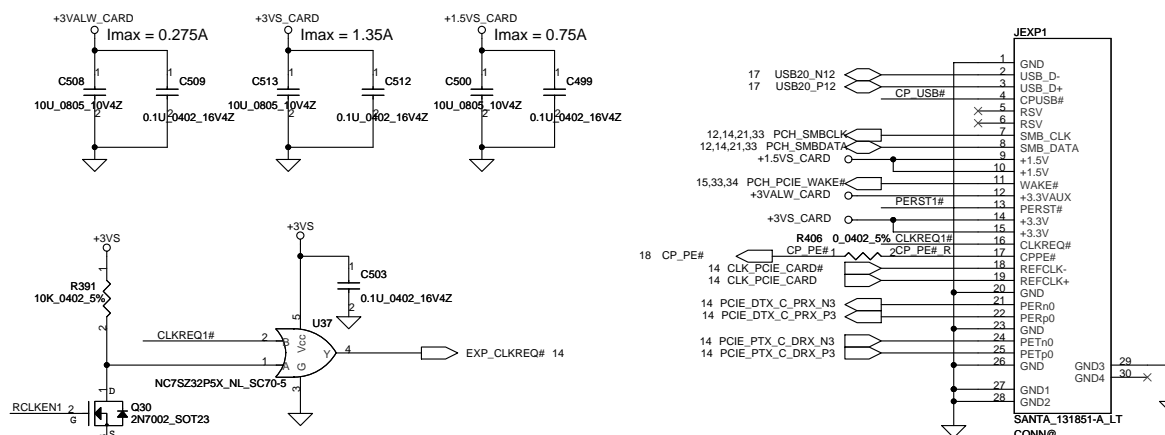


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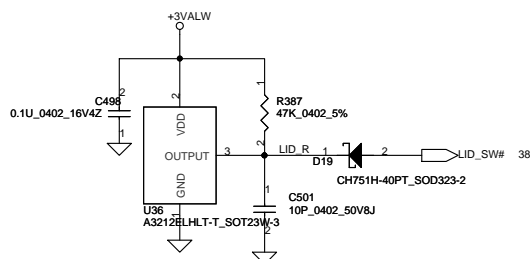
New Card Power Switch



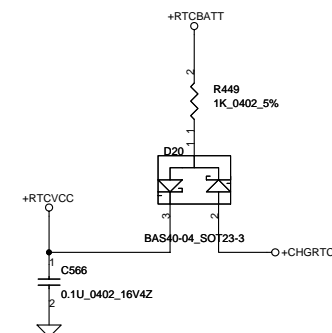
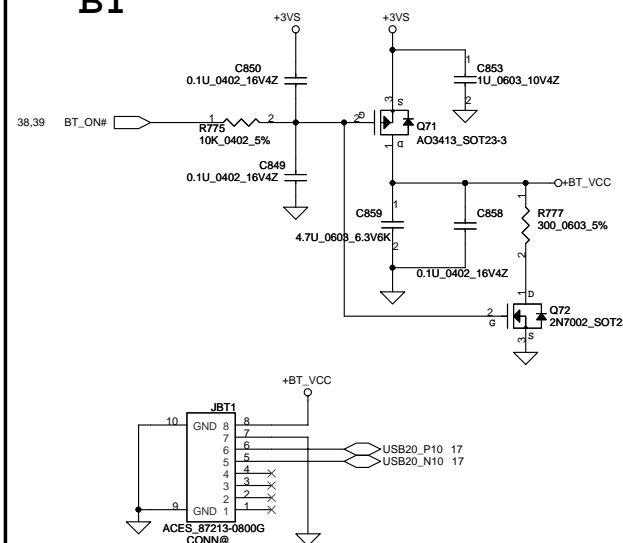
New Card Socket (Left/TOP)



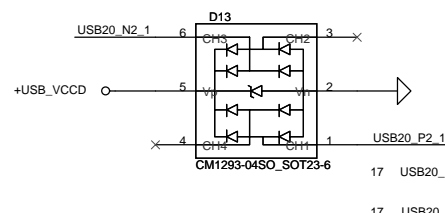
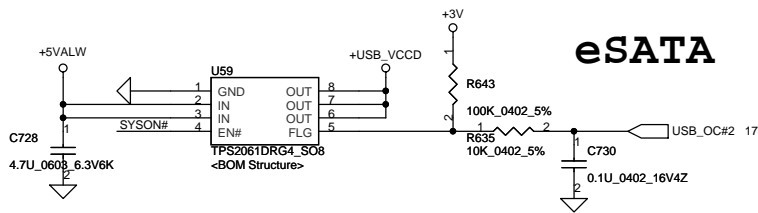
Lid Switch (Hall Effect Switch)



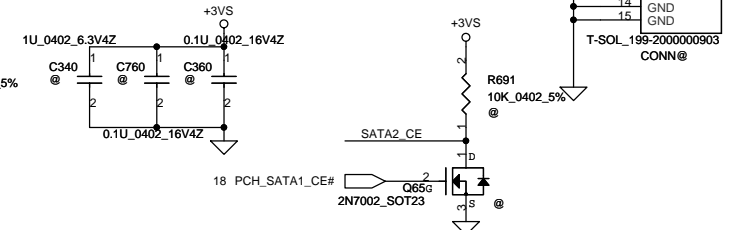
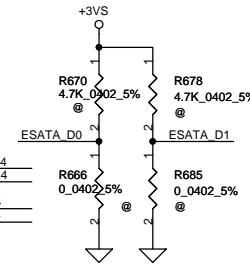
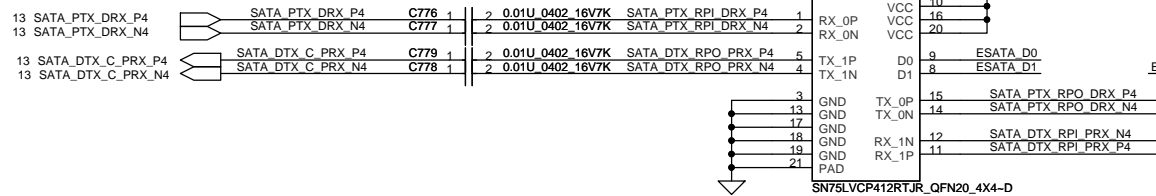
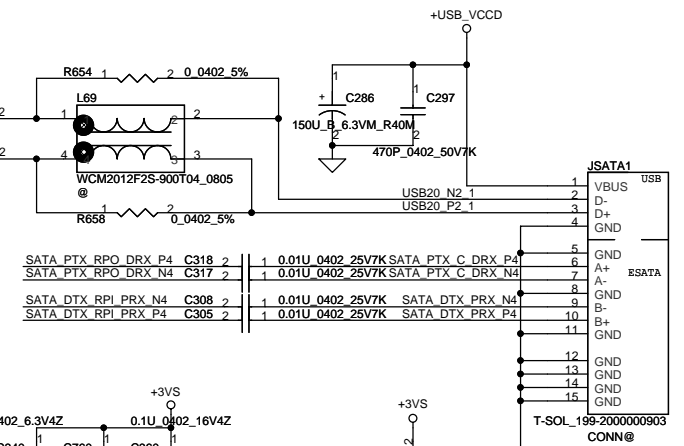
BT



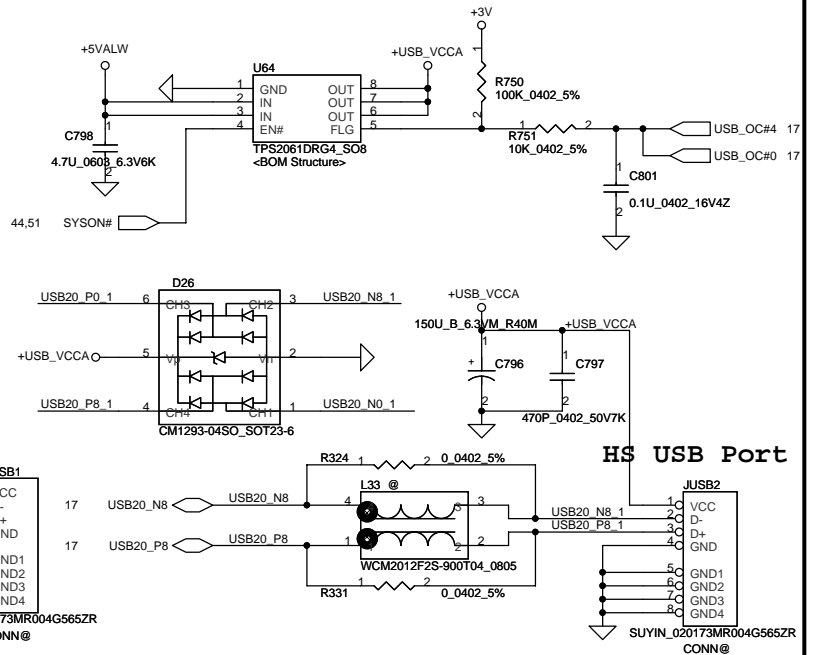
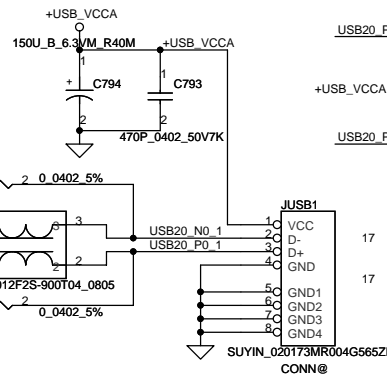
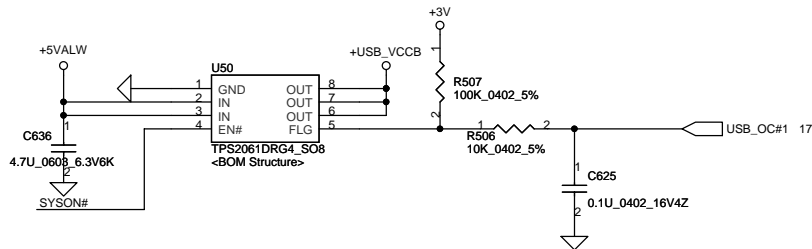
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D0	D1	Function
0	0	defalut; CH0/CH1 ->0dB
0	1	CH0->2.5dB pre-emphasis;CH1->0dB
1	0	CH1->2.5dB pre-emphasis;CH0->0dB
1	1	CH0/CH1->2.5dB pre-emphasis



USB/B & ACER LOGO Backlight Conn

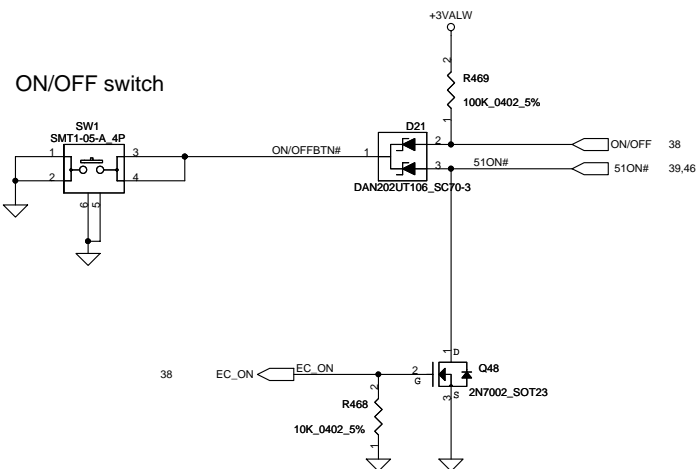


For EMI solution 02/23

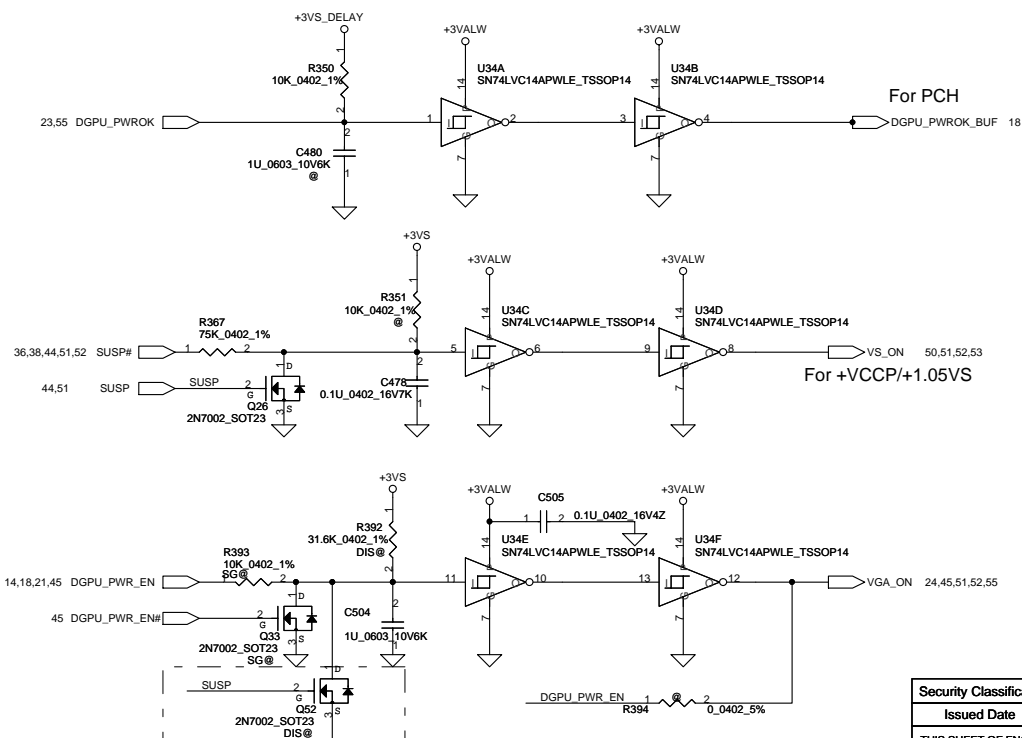
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Power Button

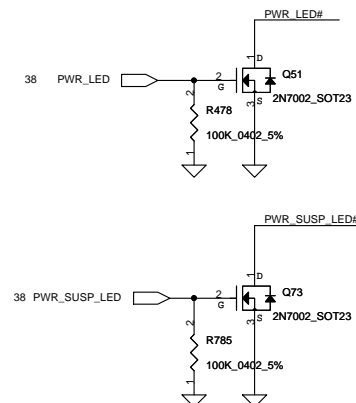


Power ON Circuit

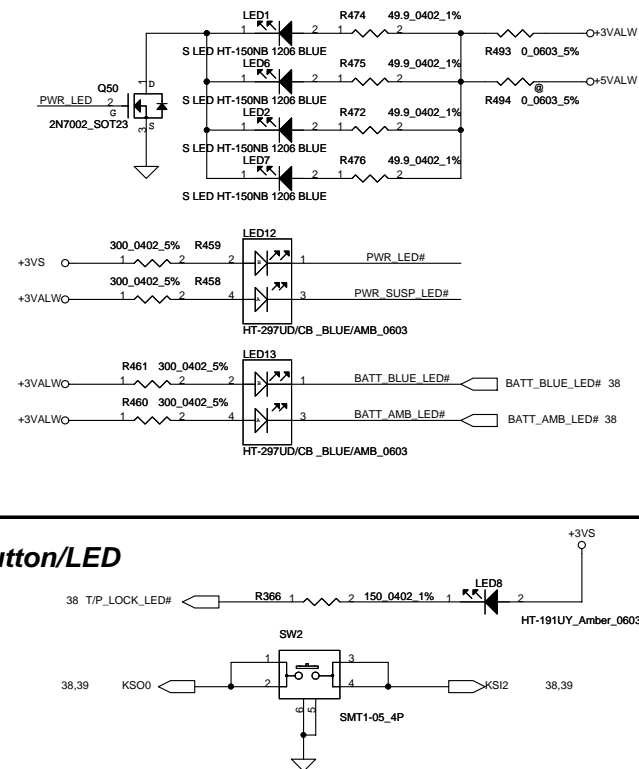


AC_IN LED

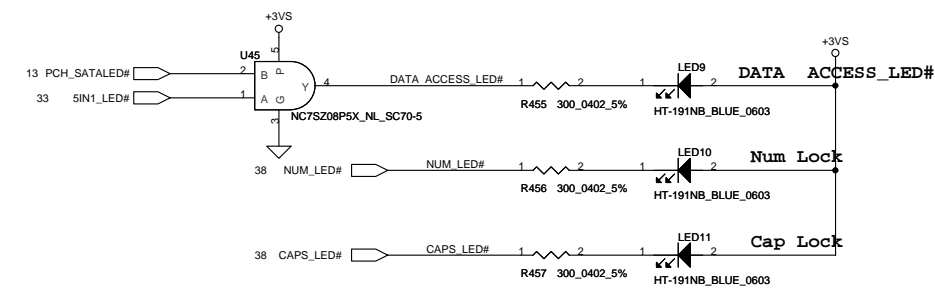
POWER LED



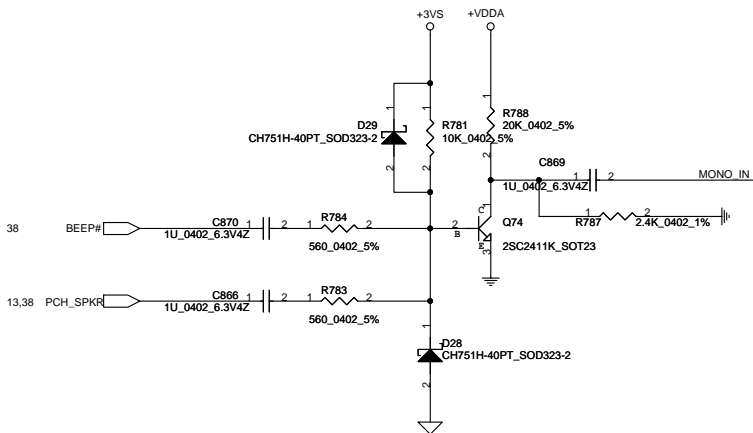
T/P Lock Button/LED



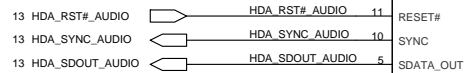
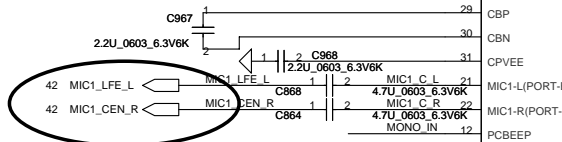
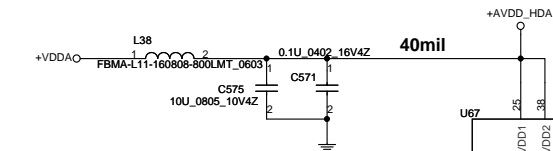
Media/Num/Cap LED



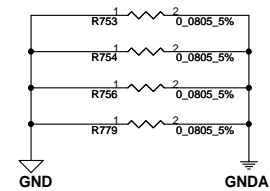
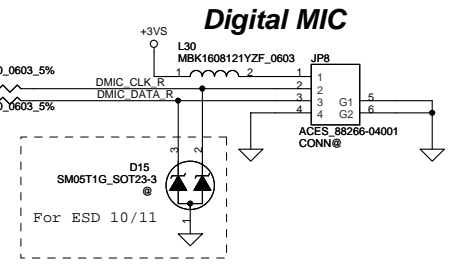
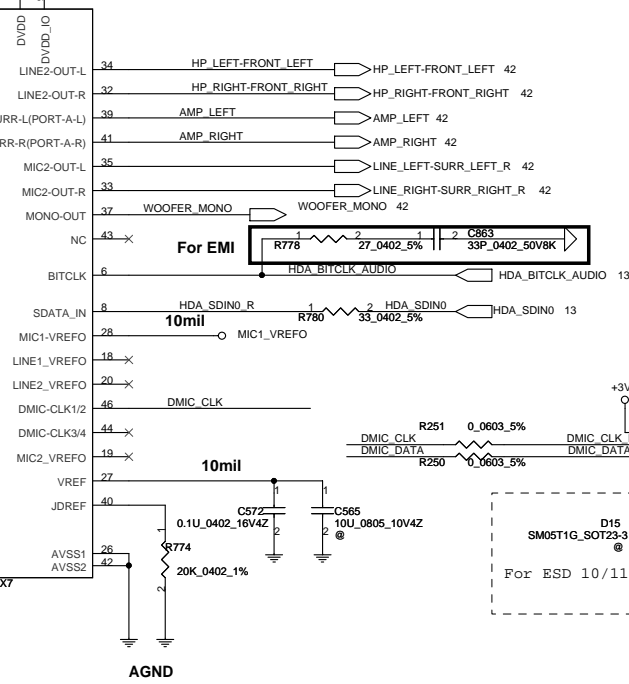
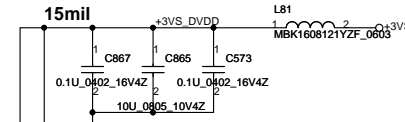
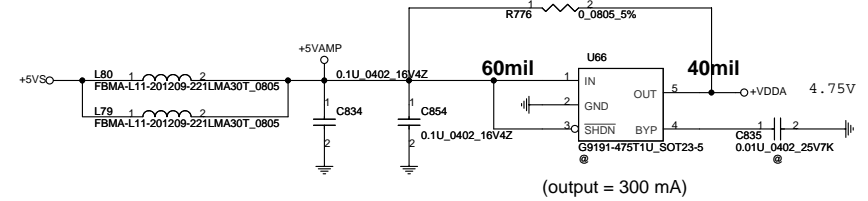
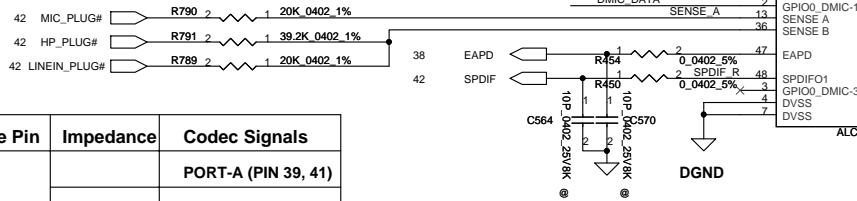
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HD Audio Codec

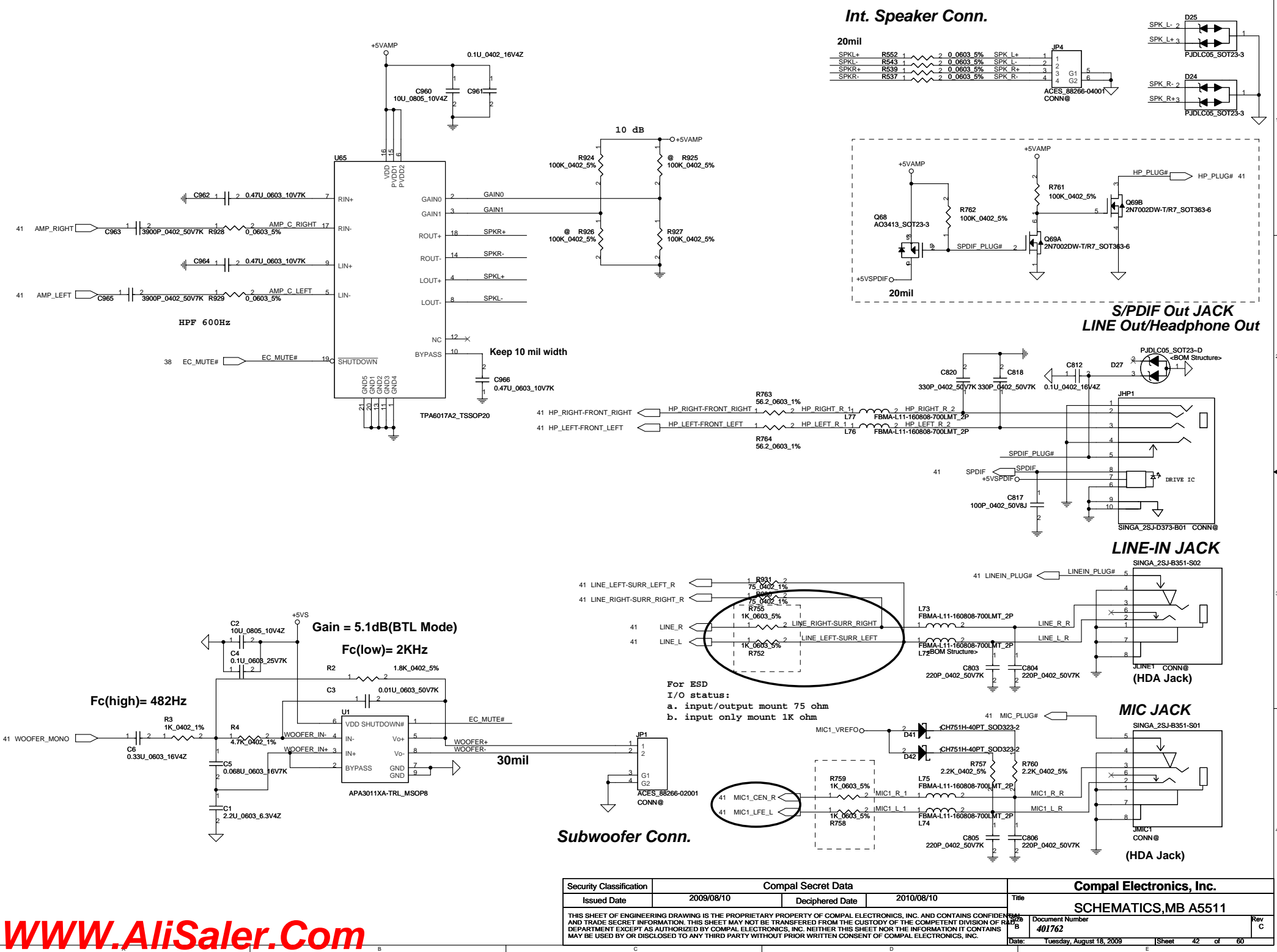


Place close to Codec



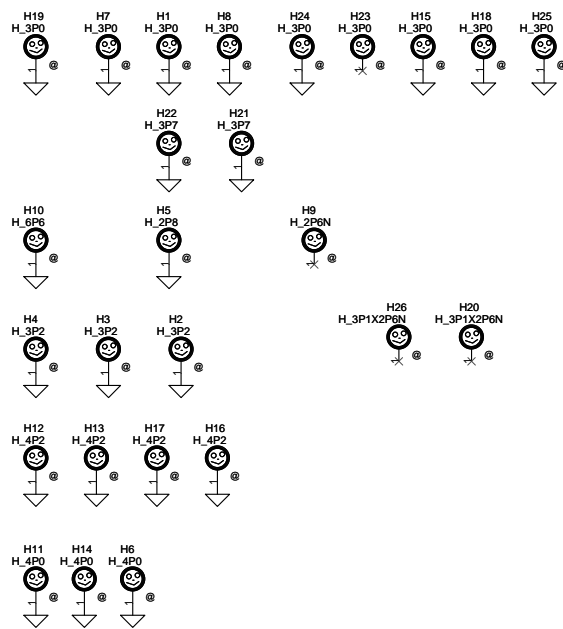
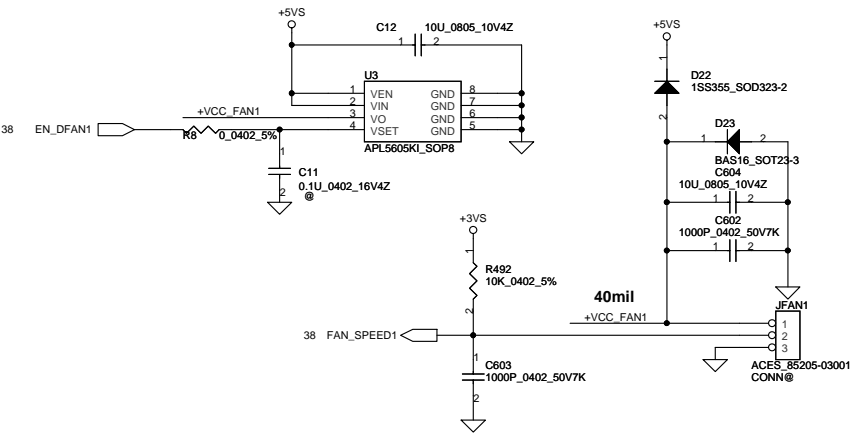
Sense Pin	Impedance	Codec Signals
SENSE A	20K	PORT-A (PIN 39, 41)
		PORT-B (PIN 21, 22)
		PORT-C (PIN 23, 24)
SENSE B	39.2K	PORT-E (PIN 32, 34)
	20K	PORT-F (PIN 33, 35)
		PORT-H (PIN 37)

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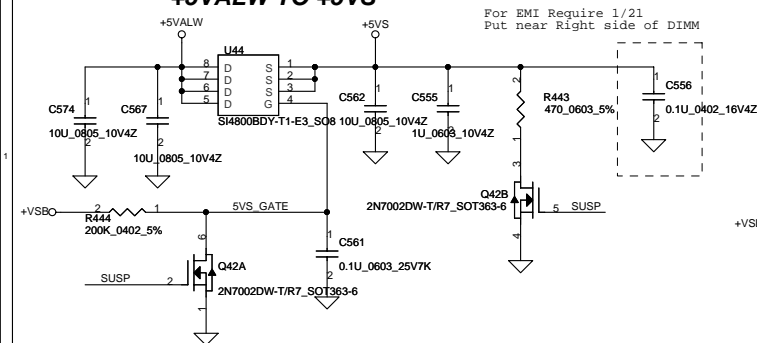
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FAN1 Conn

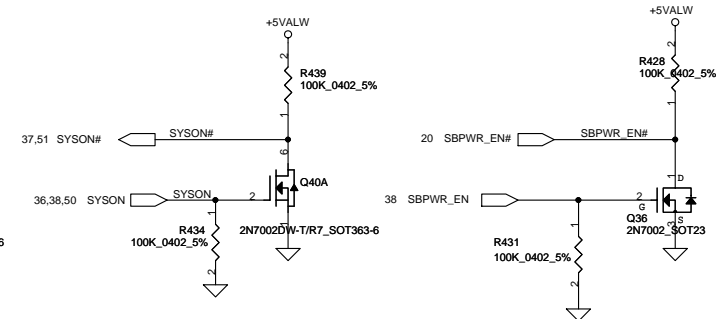
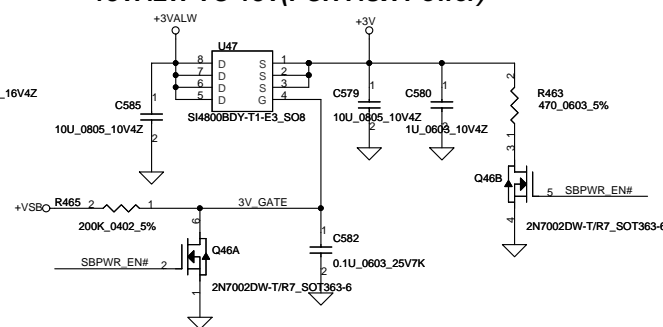


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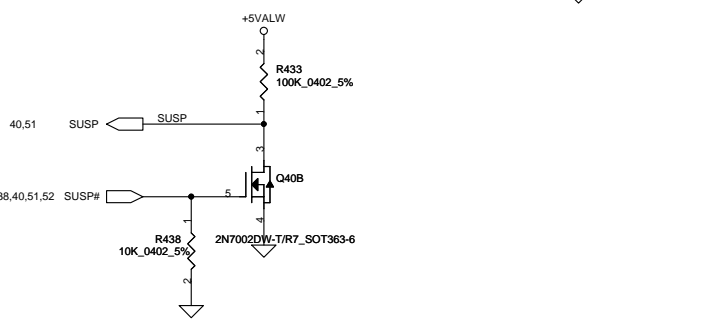
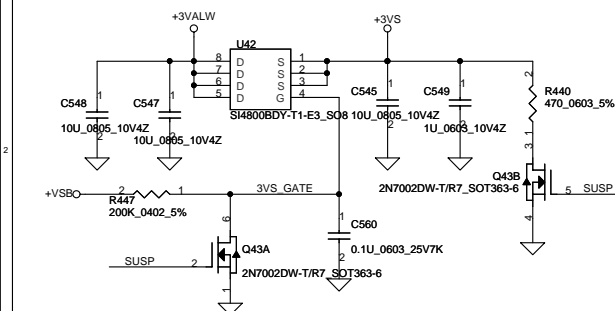
+5VALW TO +5VS



+3VALW TO +3V(PCH AUX Power)

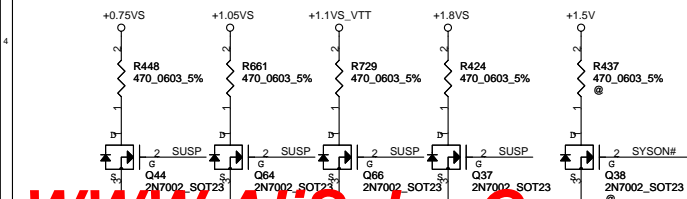
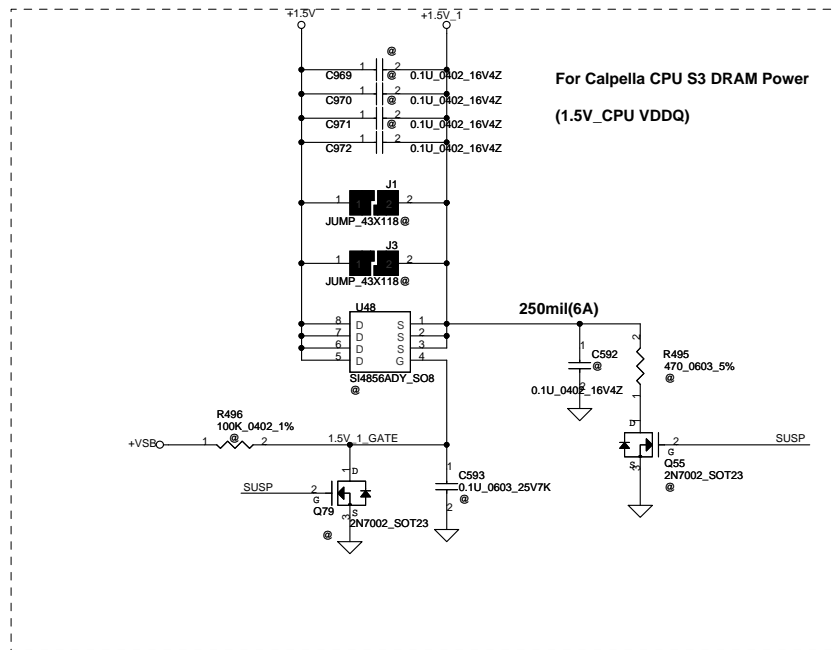
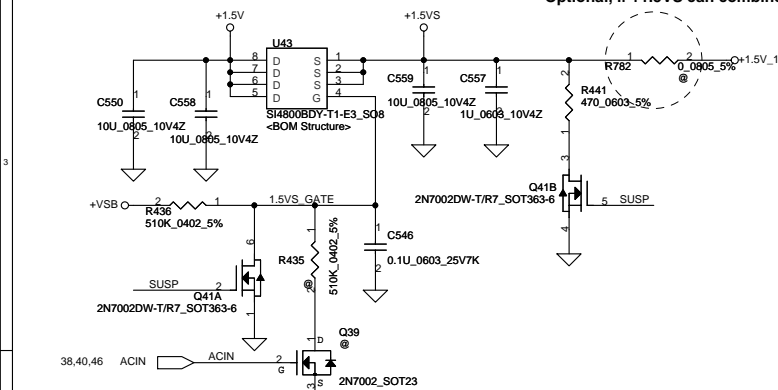


+3VALW TO +3VS



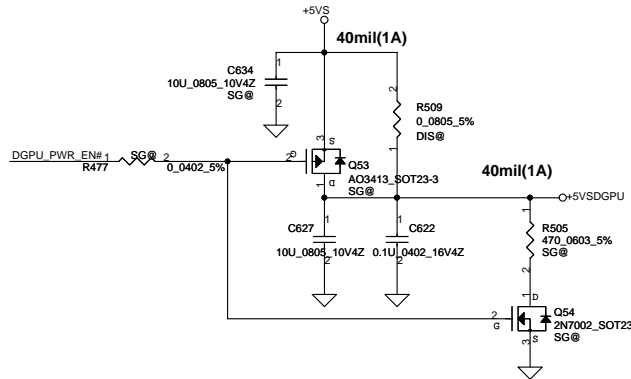
+1.5V to +1.5VS

Optional, if +1.5VS can combine with +1.5V_1

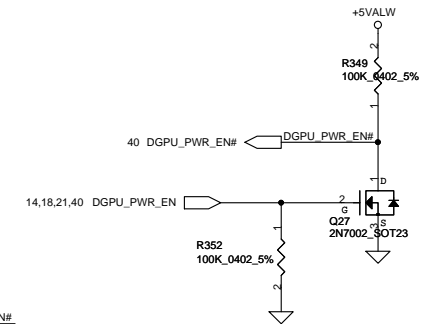
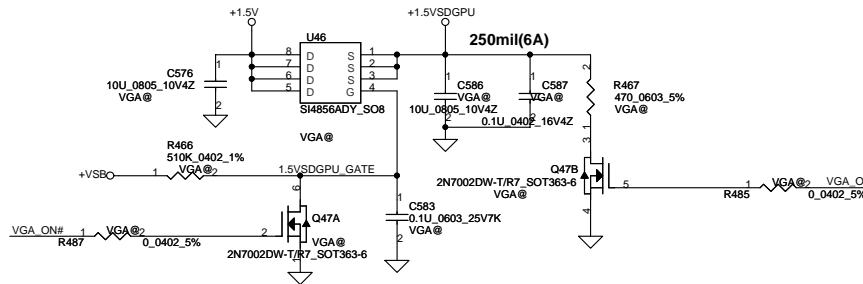


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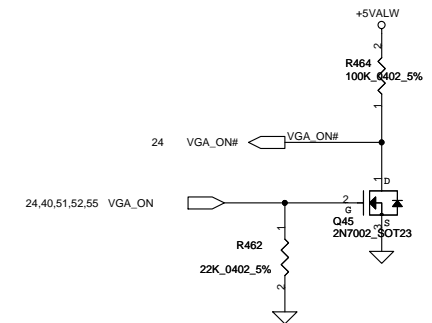
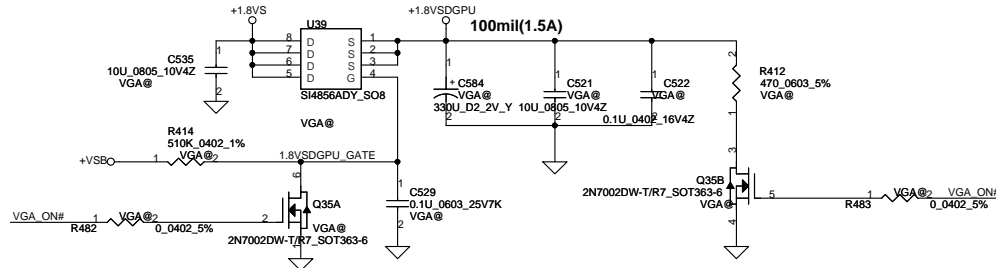
+5VS to +5VSDGPU



+1.5V to +1.5VSDGPU Transfer

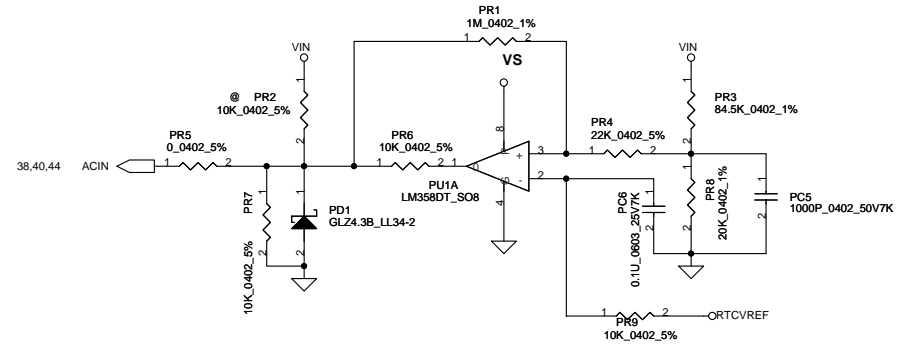
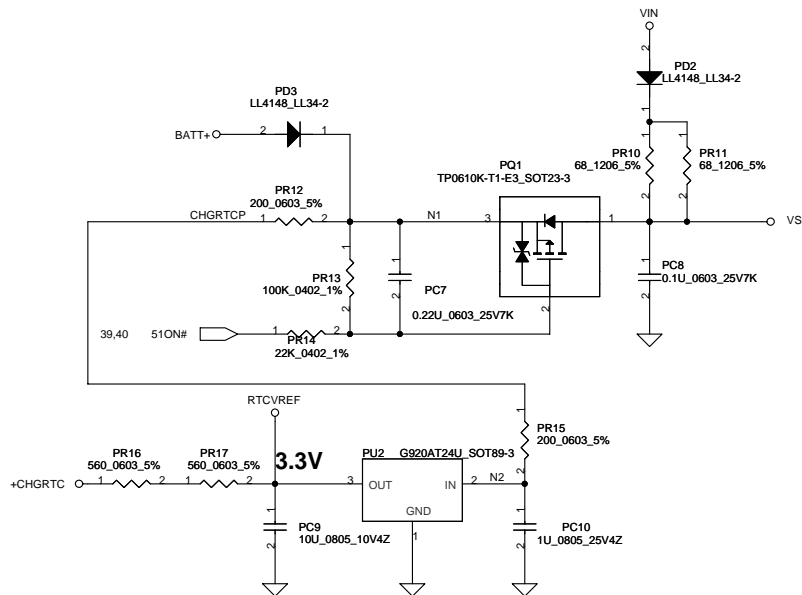
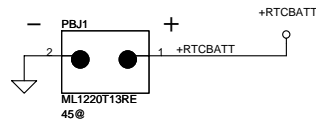
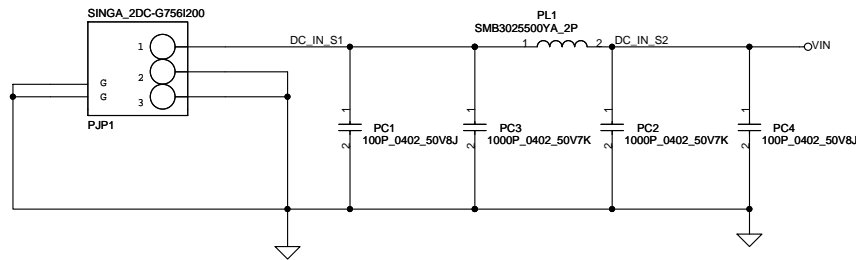


+1.8VS to +1.8VSDGPU Transfer

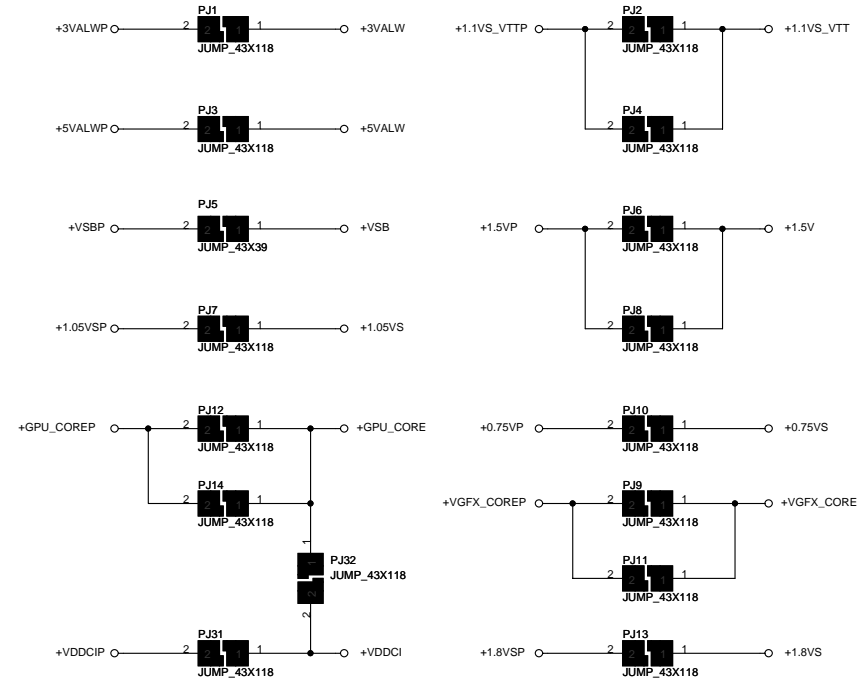


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DC231000N00 藍色 For DIS
DC231000P00 黃色 For UMA
Footprint
SINGA_2DC-S756B200_3P

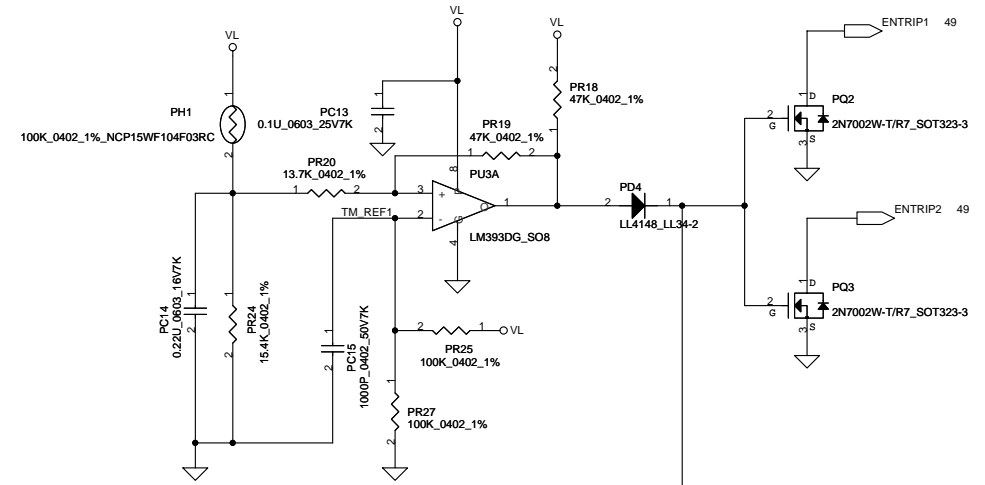
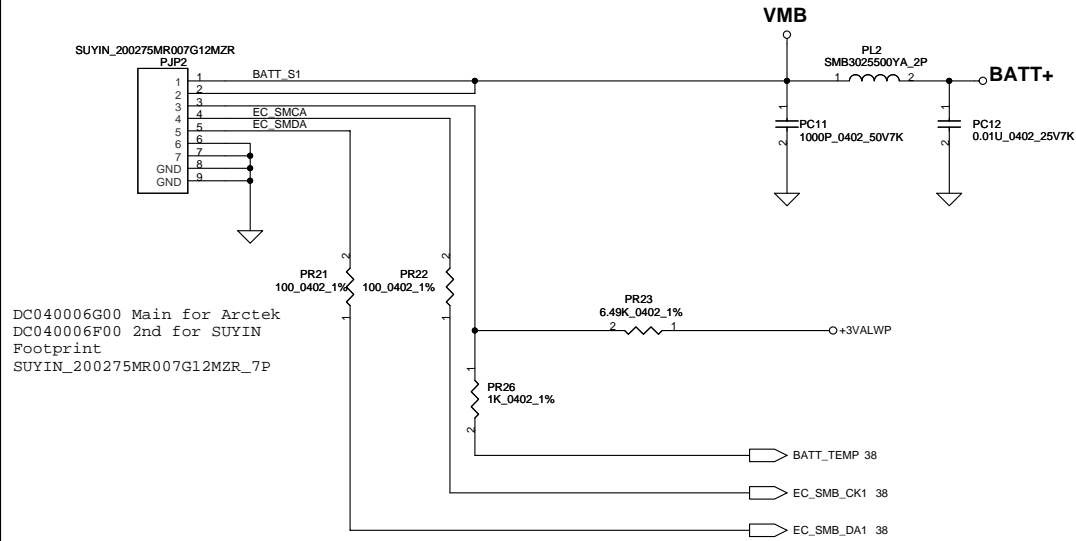


Vin Detector			
	Min.	Typ	Max.
H-->L	17.208V	17.212V	17.217V
L-->H	17.879V	17.894V	17.909V

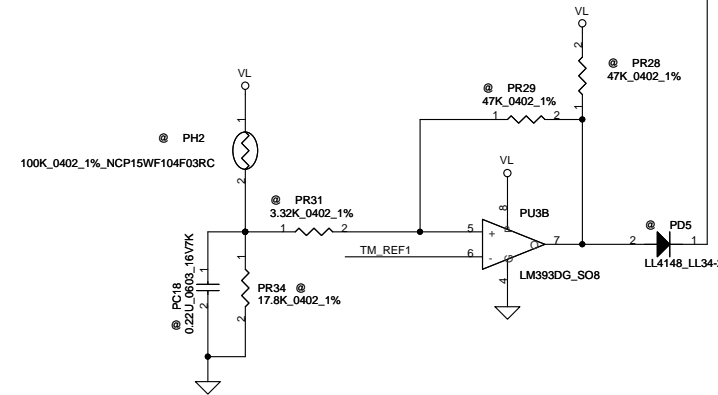
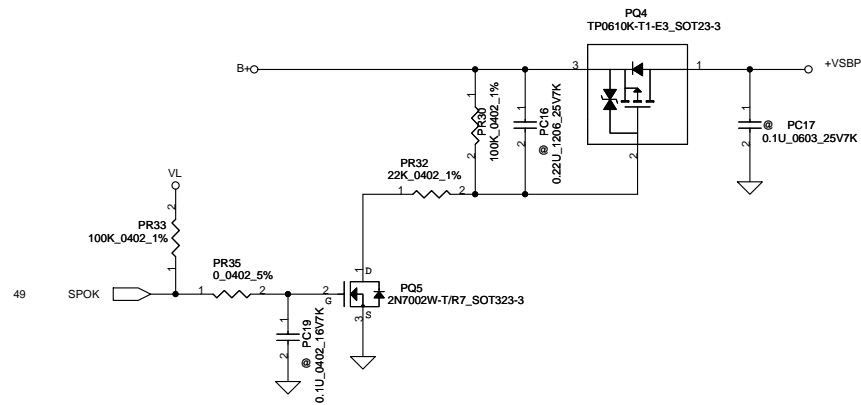


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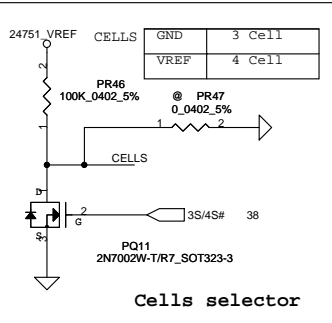
PH1 under CPU botten side :
CPU thermal protection at 92 degree C
Recovery at 56 degree C



PH2 near main Battery CONN :
BAT. thermal protection at 76 degree C
Recovery at 56 degree C

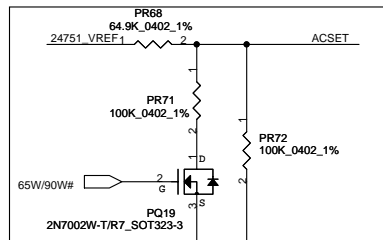


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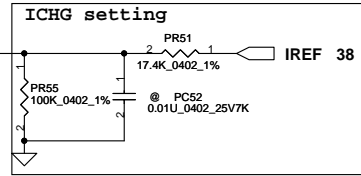
CP Point Setting
 CP point=ladapter*85%
 90W adapter
 $V_{acset}=3.3 \cdot (100K/(64.9K+100K))=2.001V$
 $CP\ Point=(V_{acset}/V_{vdac}) \cdot (0.1/PR56)=4.04A$
 65W adapter $R=(100K \cdot 100K)/(100K+100K)=50K$
 $V_{acset}=3.3 \cdot (50K/(50K+64.9K))=1.436V$
 $CP\ POINT=(1.436V/3.3V) \cdot (0.1/0.015)=2.901A$

Input OVP : 22.3V
 Input UVP : 17.26V
 Fsw : 300KHz

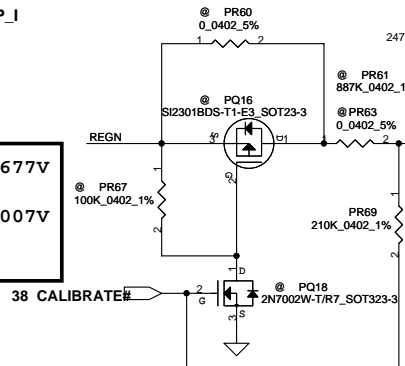


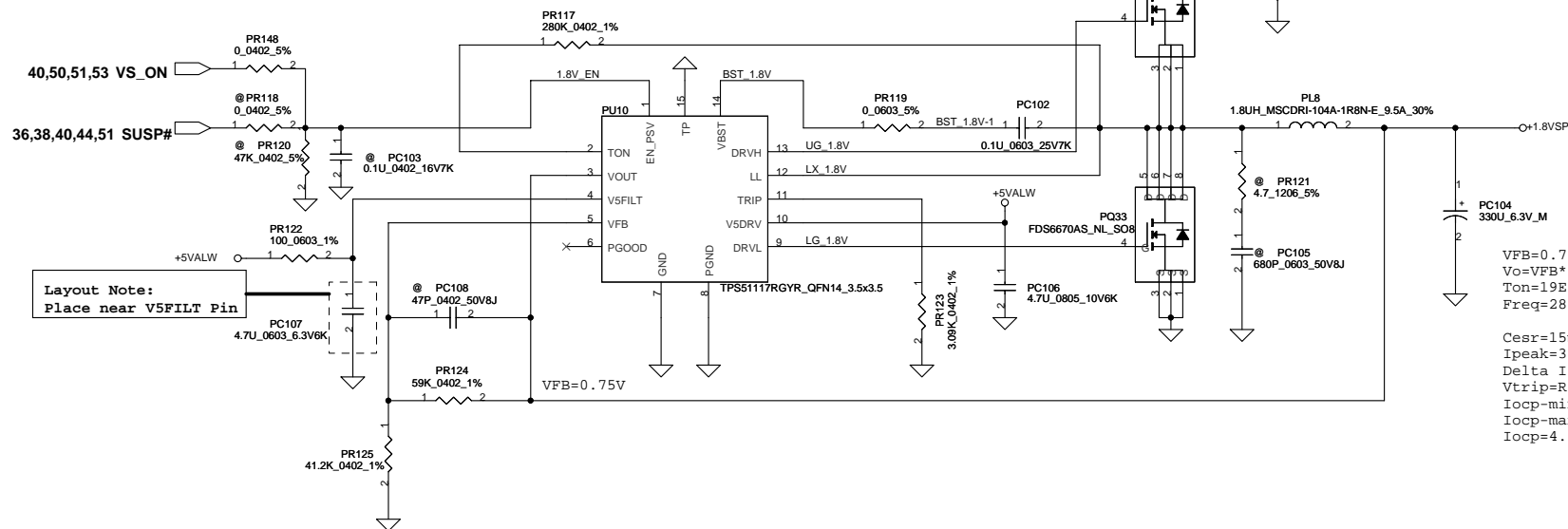
Charger ADJ	Calibrate#
4.0V	L=0V
4.2V	1.8755V
4.3V	2.8132V
4.35V	H=3.3V

LI-4S : 18.0V---BATT-OVP=2.677V
BATT-OVP=0.1487*VMB
LI-3S : 13.5V---BATT-OVP=2.007V
BATT-OVP=0.1487*VMB
Per cell=3.5V

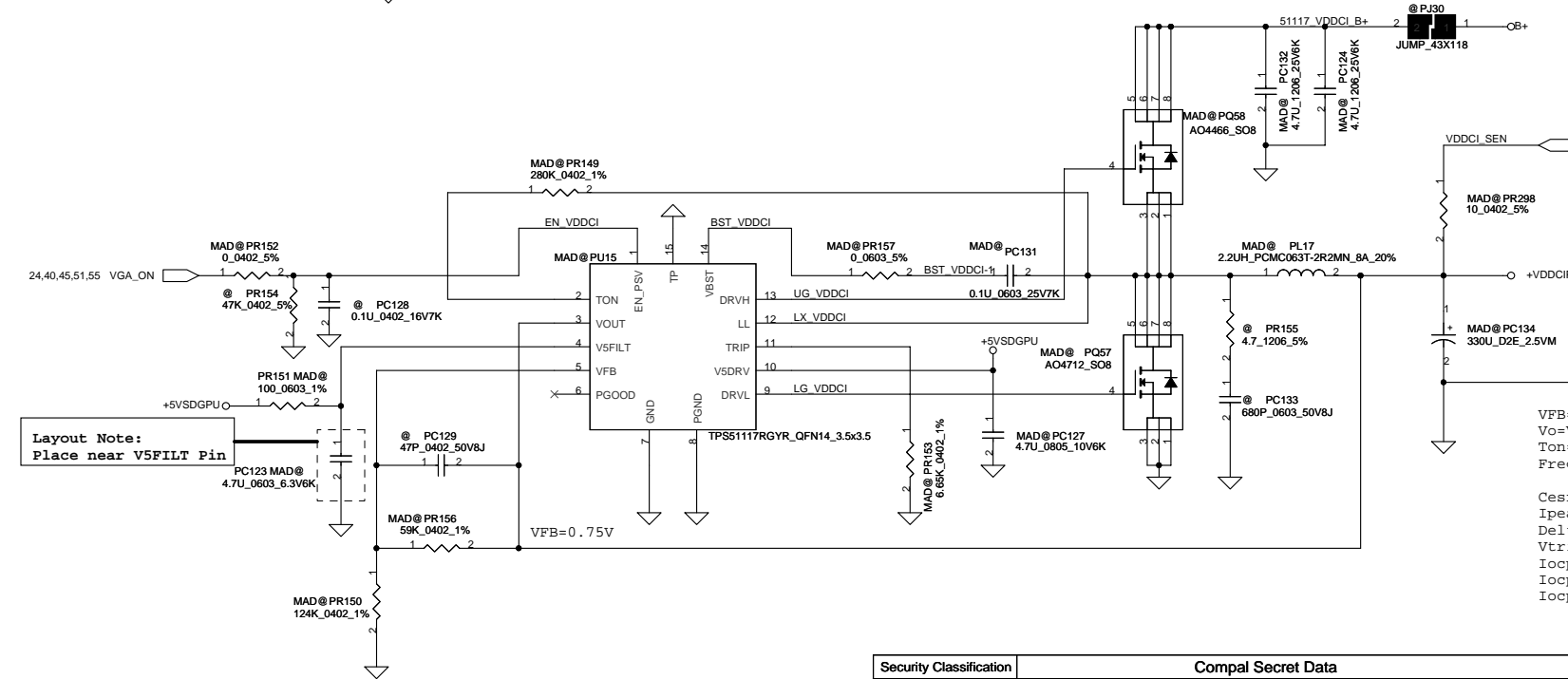


Icharge Setting
 For 2200mA, $I_{charge}=0.8C \cdot 0.8 \cdot 2 \cdot 2=3.52A$
 For 2400mA, $I_{charge}=0.8C \cdot 0.8 \cdot 2 \cdot 4=3.84A$
 $I_{charge}=(V_{acset}/V_{dac}) \cdot (0.1/PR62)$
 $IREF \cdot (100K/(100K+17.4K)/3.3) \cdot (0.1/0.02)=I_{charge}$
IREF=0.77484*Icharge





VFB=0.75V
 $V_o = VFB * (1 + PR124 / PR125) = 1.8V$
 $Ton = 19E-12 * Ron * ((2/3) * V_o + 150mV) / Vin + 50ns = 2.4E-7$
 Freq=282KHz
 Ccsr=15m ohm
 Ipeak=3.02A Imax=2.114A
 $\Delta I = ((19.5-1.5) * (1.5/19.5)) / (L * Freq) = 2.232A$
 $V_{trip} = R_{trip} * I_{ouA} = 0.0309V$
 $I_{ocp_min} = 4.60A$
 $I_{ocp_max} = 4.76A$
 $I_{ocp} = 4.60-4.76A$



VFB=0.75V
 $V_o = VFB * (1 + PR156 / PR150) = 1.1V$
 $Ton = 19E-12 * Ron * ((2/3) * V_o + 150mV) / Vin + 50ns = 2.4E-7$
 Freq=282KHz
 Ccsr=15m ohm
 Ipeak=4.00A Imax=2.80A
 $\Delta I = ((19.5-1.1) * (1.1/19.5)) / (L * Freq) = 1.67A$
 $V_{trip} = R_{trip} * I_{ouA} = 0.0665V$
 $I_{ocp_min} = 4.06A$
 $I_{ocp_max} = 5.83A$
 $I_{ocp} = 4.06-5.83A$

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Layout Note:
Place near high-side MOS Drain
and low-side MOS Source

Layout Note:
Close IC

Layout Note:
Close IC
單獨拉回不搭Pin15

Layout Note:
Close IC

Material Note:
330uF/6 mΩ, number
are 3, Power 1, HW 2

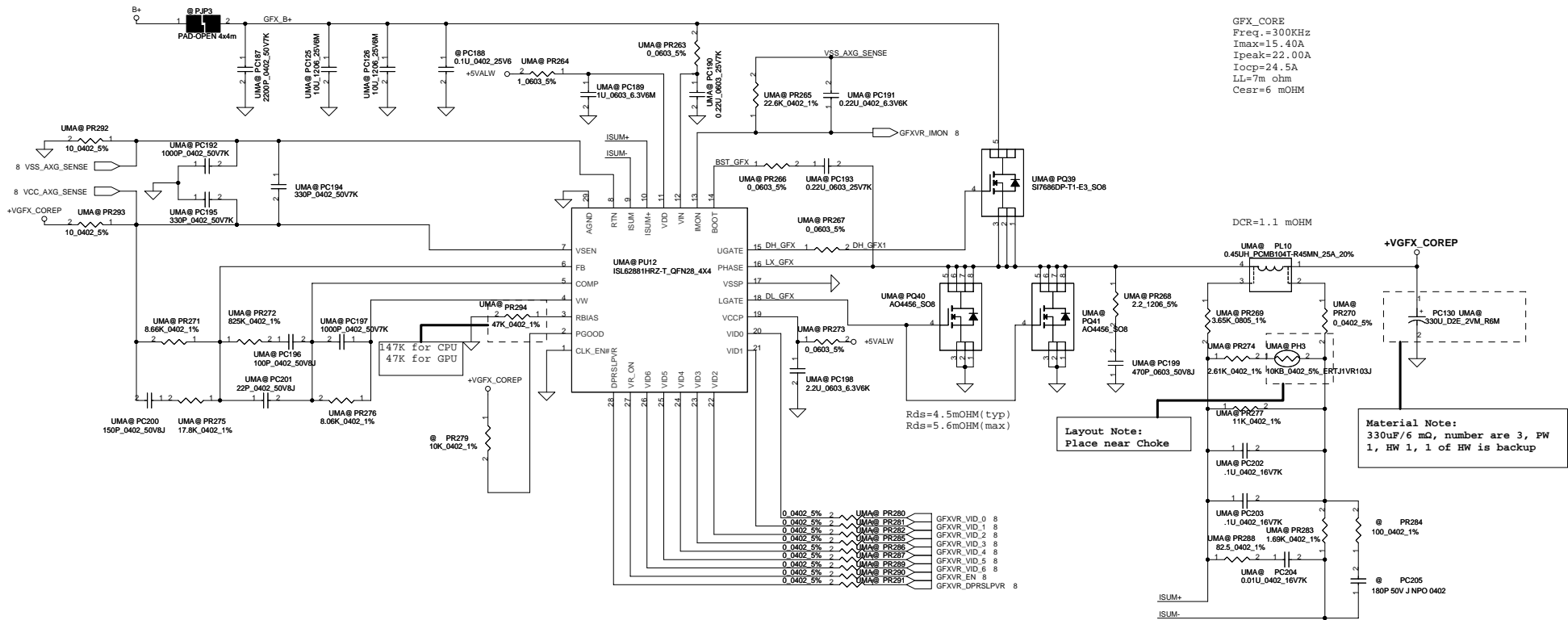
Ipeak=18.062A Imax=12.6434A
Freq.=230KHz
Iocp=20.01~27.39A

Voltage Select	
VID	Vout
High	1.05 V
Low	1.1 V

VTT Rail

Arrandale +1.1VS_VTT=1.05V
Clarksfield +1.1VS_VTT=1.1V

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Version change list (P.I.R. List)

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for PWR

Item	Fixed Issue	Reason for change	Rev.	PG#	Modify List	Date	Phase
1	BQ24751A has very low rate crack	Add BQ24751A voltage clamp protection but disable first	0.1	47	Change PR56 from 150 to 0(SD013000080) Disable PD8、PD9、PR57、PR158、PC35、PQ15	2009 05/07	EVT
2	Optimize by control IC vendor suggestion	Optimize by control IC vendor suggestion	0.1	56	Change PQ7 to power pack Disable PR236、PC177、PC185、PR262 Change PR239 from 2.26K to 2.61K(SD000009M80) Change PC179 from 0.47U to 0.047U(SE026473K80)	2009 05/11	EVT
3					Change PR256 from 1K to 1.21K(SD000004C00) Delete PR243、PR244、PR257		
4	Optimize by control IC vendor suggestion	Optimize by control IC vendor suggestion	0.1	54	Change PR271 from 10.2K to 8.66K(SD034866180) Change PC203 from 0.068U to 0.1U(SE076104KM8)	2009 05/11	EVT
5					Change PR283 from 3.01K to 1.69K(SD00000JB80) Disable PR284、PC205		
6	Tune OCP from 15.81A to 18.62A(min) & optimize compensation by control IC vendor suggestion	Tune OCP from 15.81A to 18.62A(min) & optimize compensation by control IC vendor suggestion	0.1	53	Change PR135 from 1.96K to 2.37K(SD034237180) Change PR137 from 49.9K to 90.9K(SD034909280)	2009 05/11	EVT
7	Tune VDDCI output voltage to 1.1V by HW request	Tune VDDCI output voltage to 1.1V by HW request	0.1	52	Change PR156 from 27.4K to 124K(SD034590280)	2009 05/13	EVT
8	SH16118AM00 is non lead-free part, SH16118AM10 is	SH16118AM00 is non lead-free part, SH16118AM10 is	0.1	50	Change PL7 from SH16118AM00 to SH16118AM10	2009 05/13	EVT
9	Co-layer will cause DRC, but reserve the space	Co-layer will cause DRC, but reserve the space	0.1	56	Delete PL15、PL16	2009 05/14	EVT
10	There is not enough space	Choke change size from 10x10 to 7x7	0.2	52	Change PL17 from SH000007E80 to SH000006I80	2009 05/27	EVT2
11	Tune sequence by HW request and prevent enable abnormally	Tune sequence by HW request and prevent enable abnormally	0.2	51	Change EN net from DGPU_PWR_EN# to VGA_ON Change PR116 from 47K to 22K(SD028220280)	2009 05/27	EVT2
12	Power ON while no CPU will burn out	Power ON while no CPU will burn out	0.2	53	Change Feedback from +1.1VS_VTT to +1.1VS_VTTP	2009 05/27	EVT2
13	PQ7 has very low rate crack	Change PQ7 package to TO-253 DPAK	0.2	48	Change PQ7 from AO4407 to AOD425(SB00000K800)	2009 05/27	EVT2
14	HW request	Don't need this signal	0.2	54	Delete net GFX_CORE_PWRGD	2009 06/01	EVT2
15	Optimize by control IC vendor suggestion	Optimize by control IC vendor suggestion	0.2	56	Change PR226 from 10K to 1.91K(SD000009O80) Change PR256 from 1.21K to 1.1K(SD034110180)	2009 06/01	EVT2
16	To avoid pre-charge can not finish	To avoid pre-charge can not finish	0.2	49	Add PC135 as 1U	2009 06/02	EVT2
17	To avoid 2nd source RT8209B can no power on	To avoid 2nd source RT8209B can no power on	0.2		Change PR94、PR103、PR122、PR151 from 300 to 100(SD000000080) Change PC79、PC88、PC107、PC123 from 1U to 4.7U(SE107475K80)	2009 06/02	EVT2
18	Switch delay time can't over 1mS and OCP has risk	Tune switch delay time to 1mS and OCP to 32.93A(min)	0.2	55	Change PR190 from 3.9K to 6.81K(SD034681180) Change PC151、PC152 from 0.1U to 0.22U(SE095224K00)	2009 06/02	EVT2
19	Tune OCP from 18.62A to 20.01A(min)	Tune OCP from 18.62A to 20.01A(min)	0.2	53	Change PR197 from 68.1K to 60.4K(SD034604280) Change PR135 from 2.37K to 4.02K(SD034402180)	2009 06/02	EVT2
20	Sense from VTTP and CPU both	Sense from VTTP and CPU both	0.2	53	Change PR139 to +1.1VS_VTTP Add PR160 to VTT_SENSE	2009 06/03	EVT2
21	Tune OCP to 16.47A(min) & ripple noise	Tune OCP to 16.47A(min) & ripple noise	0.2	50	Change PR95 from 13.7K to 15.8K(SD034158280) Add PC136	2009 06/08	EVT2
22	Tune Output Voltage to 1.15V(max) for batter performance by HW request	Tune Output Voltage to 1.15V(max) for batter performance by HW request	0.3	55	Change PR196 from 9.76K to 7.32K(SD034732180) Change PR297 from 0 to 10(SD028100A80)	2009 06/17	EVT3
23	Tune CPU transient	Tune CPU transient	0.3	56	Change PC179 from 47nF to 68nF(SE026683K80)	2009 06/17	EVT3

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A1--> A2 Change List

2009/05/26
Page 33 SWAP HDD SATA_DTX_C_PRX_N1/P1
Page 38 Del DPIO42 (GFX_CORE_PWRGD) and ADD ME_EN in GPIO42 to PCH GPIO33 (For enable ME to entry manufactruing mode)
Page 12/37 Del PCH_SATA2_CE# and change PCH_SATA1_CE# for Esata redriver IC enable singal

2009/06/02
Page 30 Reverse JLVDS1 pin 36 and pin 37
Page 39 Reverse JKBl pin defined
Page 12 colay Relatek CLK Gen
Page 39 Follow EMI request,add R486 and C9...
Page 24 switch the net name EC_SMB_DA2 and EC_SMB_CK2

2009/06/03
Page 40 add R490,R491,R493 and R494 for LED brightness
Page 38 change EC pin 75 from GFX_CORE_PWRGD to ME_EN

2009/06/04
change Y1,Y3,Y4,Y10,X1 crystal PCB footprint
Page 45 change R462 to 22k
Page 15 change R315 to 100k

A2--> A3 Change List

2009/06/25
Page 14 R305 pull high to +3VS_Delay
Page 15,24,38 Add ACIN_BUF for PCH/VGA
Page 24 Un-pop R177 (No use external Vbios ROM)
change R28 to 510K (for VGA Power on sequence)
Page5,6,7,44 Reserve INTEL Capella new design schematic
Page 24 SWAP Q57,Q58,Q62 Pinl and PIN3,
change Q62 to UMA@
Page 38 change PWR_SUSP_LED to U38.84
Page 36,38,39 combine LED fuction to BT_ON#
Page 39 SWAP JP9
Page 40 Add discharge schematic for VGA_ON

A3-->C Change List

2009/07/06
Page 32 Switch the U57 Pin 27 and Pin 49 (IGPU_SELECT# and DGPU_SELECT#)

2009/07/08
Page 24 Add R833,for short +3VS to +3VS_DELAY
Page 25 Add R116 and R225 for Boradway MVREFDA/B and MVREFSA/B
Page 25 Add C473,C474,R265 and R327 for Boradway CLKTESTA/B
Page 27 Add R770 and R771
Page 32 Add R768,R769,R767,R786,R772 and Delete Q62,R793 to verify HDMI HPD
Page 18 Add R333 to pull down GPIO37 and change R293 to UMAO@

2009/07/10
change 4.7u_0805 to 4.7u_0603
Page 14 Add R104,R793,R342 and R341 for PEG_CLKREQ#
Page 38 update Board ID to 0.4 R364=100K,R365=56K

2009/07/13
Page 25 add R343,R344,R361,R498,R499 and R500 for broadway
Page 7 update 470uF to 330uF(C232, C186, C711, C221, C259 and C196)
Page 39 Update R5 and R6 package from 0402 to 0603...
Page 24 add Q76,C476 and R795 for +3VS_DELAY
Page 24 Switch Q9 and change the +3VS to +3VS_DELAY

C-->Pre-MP Change List

2009/07/17
Page 42 switch MIC1_LFE_L and MIC1_CEN_R

2009/07/28
Page 39 Add Q62 to replace D11
Page 25 Add R502 and R504

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MODEL NAME: *KBLA0 Power Sequence Block Diagram*
PCB NAME: *LA4811P*
REVISION:
DATE: *2008/12/04*

